Exhibit 25

National Semiconductor

LVDS Owner's Manual

A General Design Guide for National's Low Voltage Differential Signaling (LVDS) and Bus LVDS Products

Moving Info with LVDS

2nd Edition

Revision 2.0 — Spring 2000

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LVDS Owner's Manual

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Introduction to LVDS

Chapter 1

1.0.0 INTRODUCTION TO LVDS

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces or a balanced cable.

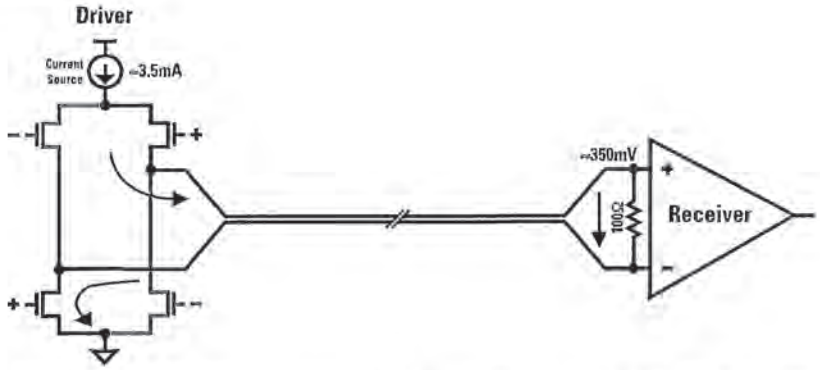
1.1.0 THE TREND TO LVDS

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics and photo-realistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high-speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from board-to-board or box-to-box, however, requires an extremely high-performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise and is inexpensive. Unfortunately existing solutions are a compromise of these four basic ingredients: **performance, power, noise, and cost.**

1.2.0 GETTING SPEED WITH LOW NOISE AND LOW POWER

LVDS is a low swing, differential signaling technology which allows single channel data transmission at hundreds or even thousands of Megabits per second (Mbps). Its low swing and current-mode driver outputs create low noise and provide very low power consumption across frequency.

1.2.1 How LVDS Works



Simplified Diagram of LVDS Driver and Receiver Connected via 100Ω Differential Impedance Media

National's LVDS outputs consist of a current source (nominal 3.5mA) which drives the differential pair line. The basic receiver has high DC input impedance, so the majority of driver current flows across the 100Ω termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

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1.2.2 Why Low Swing Differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers which looks at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. And, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low — almost flat — power consumption across frequency is obtained. Switching spikes in the driver are very small, so that I_{CC} does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5mA x 350mV = 1.2mW) is very small in magnitude.

1.2.3 The LVDS Standard

LVDS is currently standardized by two different standards:

TIA/EIA (Telecommunications Industry Association/Electronic Industries Association)
- ANSI/TIA/EIA-644 (LVDS) Standard

IEEE (Institute for Electrical and Electronics Engineering)
- IEEE 1596.3

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644 (LVDS) Standard
Note: Actual datasheet specifications may be significantly better.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change to V_{OD}|		50	|mV|
ΔV_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short Circuit Current		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)	0.26	30% of t_{ui}†	ns
I_{IN}	Input Current		20	|μA|
V_{TH}	|Threshold Voltage|		±100	mV
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e. bit width).

The ANSI/TIA/EIA standard notes a recommend a maximum data rate of 655Mbps (based on one set of assumptions) and it also provides a theoretical maximum of 1.923Gbps based on a loss-less medium. This allows the referencing standard to specify the maximum data rate required depending upon required signal quality and media length/type. The standard also covers minimum media specifications, failsafe operation of the receiver under fault conditions, and other configuration issues such as multiple

receiver operation. The ANSI/TIA/EIA-644 standard was approved in November 1995. National Semiconductor held the editor position for this standard and chairs the sub committee responsible for electrical TIA interface standards. Currently the 644 spec is being revised to include additional information about multiple receiver operation. The revised (to be known as TIA-644-A) is expected to be balloted upon in calendar year 2000.

The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the IEEE 1596.3 standard. The SCI-LVDS standard also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB traces or cable, thereby serving a broad range of applications in many industry segments.

1.2.4 A Quick Comparison between Differential Signaling Technologies

Parameter	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2 to ±5 V	±600-1000mV	±250-450mV
Receiver Input Threshold	±200mV	±200-300mV	±100mV
Data Rate	<30Mbps	>400Mbps	>400Mbps

Parameter	RS-422	PECL	LVDS*
Supply Current Quad Driver (no load, static)	60mA (max)	32-65mA (max)	8.0mA
Supply Current Quad Receiver (no load, static)	23mA (max)	40mA (max)	15mA (max)
Propagation Delay of Driver	11ns (max)	4.5ns (max)	1.7ns (max)
Propagation Delay of Receiver	30ns (max)	7.0ns (max)	2.7ns (max)
Pulse Skew (Driver or Receiver)	N/A	500ps (max)	400ps (max)

*LVDS devices noted are DS90LV047A/048A

The chart above compares basic LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are one-tenth of RS-422 and also traditional TTL/CMOS levels. Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

1.2.5 Easy Termination

Whether the LVDS transmission medium consists of a cable or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed (edge rates) signals. If the medium is not properly terminated, signals reflect from the end of the cable or trace and may interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions and provides the optimum signal quality.

To prevent reflections, LVDS requires a terminating resistor that is matched to the actual cable or PCB traces differential impedance. Commonly 100Ω media and terminations are employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input.

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The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL can require more complex termination than the one-resistor solution for LVDS. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ω resistor across the receiver input.

1.2.6 Maximum Switching Speed

Maximum switching speed of a LVDS Interface is a complex question, and its answer depends upon several factors. These factors are the performance of the Line Driver (Edge Rate) and Receiver, the bandwidth of the media, and the required signal quality for the application.

Since the driver outputs are very fast, the limitation on speed is commonly restricted by:

1. How fast TTL data can be delivered to the driver – in the case of simple PHY devices that translate a TTL/CMOS signal to LVDS (i.e. DS90LV047A)

2. Bandwidth performance of the selected media (cable) – type and length dependent

In the case of LVDS drivers, like the DS90LV047A, its speed is limited by how fast the TTL data can be delivered to the driver.

National's Channel Link devices capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream — more about this later.

1.2.7 Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination, for 90mW power consumption — 75 times more than LVDS.

LVDS devices are implemented in CMOS processes, which provide low static power consumption. The circuit design of the drivers and receiver require roughly one-tenth the power supply current of PECL/ECL devices (quad device comparison).

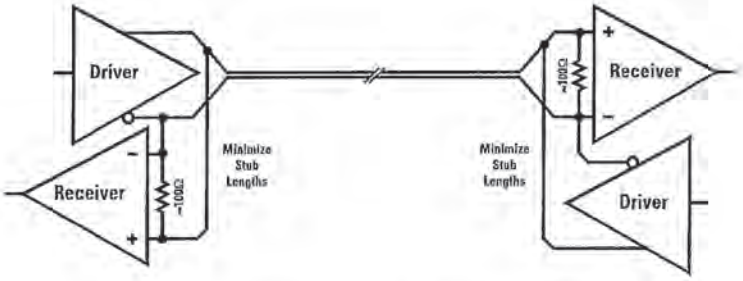
Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power through its current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. Frequency plot for LVDS is virtually flat between 10MHz and 100MHz for the quad devices (DS90C031/2), <50mA total for driver and receiver at 100MHz. Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

1.2.8 LVDS Configurations

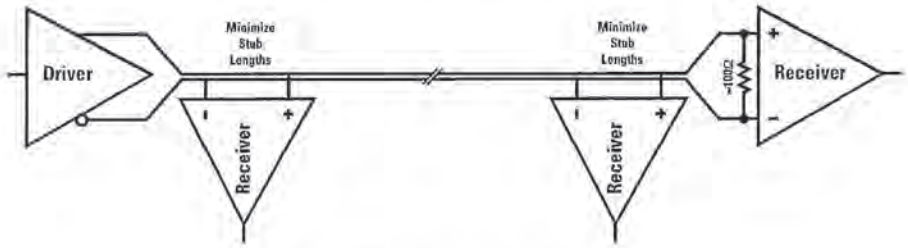
Point-to-Point Configuration

LVDS drivers and receivers are commonly used in a point-to-point configurations as shown above. However, other topologies/configurations are also possible.

The configuration shown next allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (<10m). (See also Bus LVDS Devices (Chapter 6) - which are designed for double termination loads and provide full LVDS compatible levels).



Bi-Directional Half-Duplex Configuration



Multidrop Configuration

A multidrop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than12mm – application dependent). (See also Bus LVDS Devices, which are designed for double termination loads and provide LVDS compatible levels)

Dedicated point-to-point links provide the best signal quality due to the clear path they provide. LVDS has many advantages that make it likely to become the next famous data transmission standard for data rates from DC to hundreds of Mbps and short haul distances in the tens of meters. In this role, LVDS will far exceed the 20Kbps to 30Mbps rates of the common RS-232, RS-422, and RS-485 standards.

1.3.0 AN ECONOMICAL INTERFACE - SAVE MONEY TOO

LVDS can save money in several important ways:

1. National's LVDS solutions are inexpensive CMOS implementations as compared to custom solutions on elaborate processes.
2. High performance can be achieved using low cost, off-the-shelf CAT3 cable and connectors, and/or FR4 material.
3. LVDS consumes very little power, so power supplies, fans, etc. can be reduced or eliminated.
4. LVDS is a low noise producing, noise tolerant technology – power supply and EMI noise headaches are greatly minimized.
5. LVDS transceivers are relatively inexpensive and can also be integrated around digital cores providing a higher level of integration.
6. Since LVDS can move data so much faster than TTL, multiple TTL signals can be serialized or mux'ed into a single LVDS channel, reducing board, connector, and cable costs.

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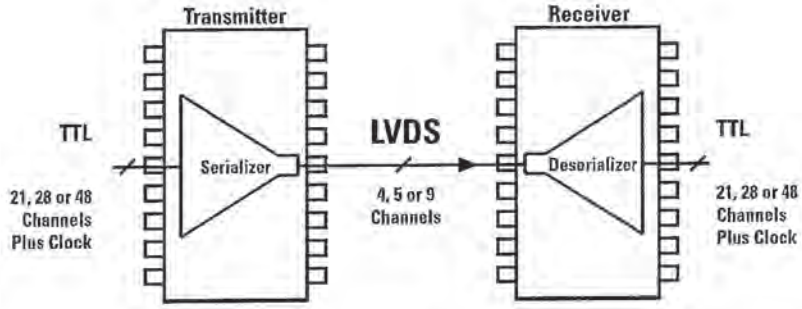

National's Channel Link Chipsets Convert a TTL Bus into a Compact LVDS Data Stream and Back to TTL.

In fact, in some applications, the PCB, cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic (user-friendly) system.

1.4.0 LVDS APPLICATIONS

The high-speed and low power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	(Box-to-box & rack-to-rack)	
Multimedia peripheral links		

1.5.0 NATIONAL'S WIDE RANGE OF LVDS SOLUTIONS

National Semiconductor offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV047A/DS90LV048A quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains singles, duals and quad footprints.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI) devices. These parts provide a high bandwidth, low power, small size, low power interface enabling XGA/SXGA/UXGA and beyond displays for notebook and monitor applications.

Another more generalized use of LVDS is in the National Channel Link family, which can take 21, 28 or 48-bits of TTL data and converts it to 3, 4 or 8 channels of LVDS data plus LVDS clock. These devices provide fast data pipes (up to 5.4 Gbps throughput) and are well suited for high-speed network hubs or routers applications or anywhere a low cost, high-speed link is needed. Their serializing nature provides an overall savings to system cost as cable and connector physical size and cost are greatly reduced.

Bus LVDS is an extension of the LVDS Line drivers and receivers family. They are specifically designed for multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30 to 50Ω range. Bus LVDS drivers provide about 10mA of output current so that they provide

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LVDS swings with heavier termination loads. Transceivers and Repeaters are currently available in this product family. A 10-bit Serializer and Deserializer family of devices is available that embeds and recovers clock from a single serial stream. This chip set also provides a high level of integration with on-chip clock recovery circuitry. Certain Deserializers provide a random data lock capability (An Industry First). The Deserializer can be hot-plugged into a live data bus and does not require PLL training.

Special Functions are also being developed using LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs is available (DS92CK16) and also a line of crosspoint switches is being introduced.

Over 75 different LVDS products are currently offered by National. For the latest in product information, and news, please visit National's LVDS web site at: **www.national.com/appinfo/lvds/**

1.6.0 CONCLUSION

National's LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.

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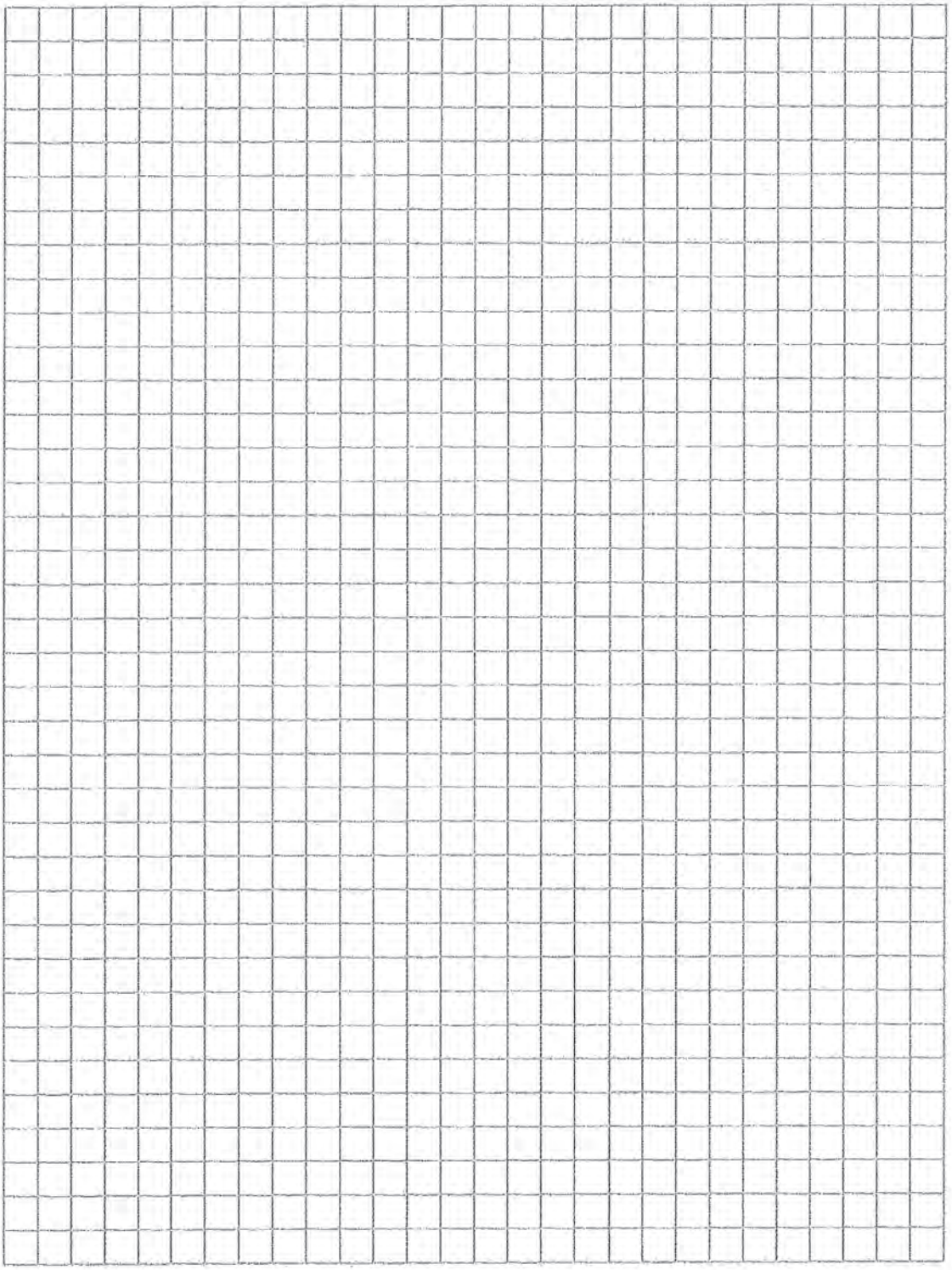
NOTES



LVDS Advantages

Chapter 2

2.0.0 LVDS ADVANTAGES

2.1.0 LVDS ELECTRICAL CHARACTERISTICS

LVDS current-mode, low-swing outputs mean that LVDS can drive at high-speeds (up to several hundred or even thousands of Mbps over short distances). If high-speed differential design techniques are used, signal noise and electromagnetic interference (EMI) can also be reduced with LVDS because of:

1. The low output voltage swing (≈350mV)
2. Relatively slow edge rates, dV/dt ≈ 0.300V/0.3ns = 1V/ns
3. Differential (odd mode operation) so magnetic fields tend to cancel
4. "Soft" output corner transitions
5. Minimum I_{CC} spikes due to low current-mode operation

LVDS can be designed using CMOS processes, allowing LVDS to be integrated with standard digital blocks. LVDS can be used in commercial, industrial, and even military temperature ranges and operate from power supplies down to 2 volts. LVDS uses common copper PCB traces and readily available cables and connectors as transmission media, unlike fiber optics.

Presently the major limitations of LVDS are its point-to-point nature (as opposed to multipoint – see Bus LVDS) and short transmission distance (10-15m), where other technologies must presently be used.

Advantages	LVDS	PECL	Optics	RS-422	GTL	TTL
Data rate up to 1Gbps	+	+	+	-	-	-
Very low skew	+	+	+	-	+	-
Low dynamic power	+	-	+	-	-	-
Cost effective	+	-	-	+	+	+
Low noise/EMI	+	+	+	-	-	-
Single power supply/reference	+	-	+	+	-	+
Migration path to low voltage	+	-	+	-	+	+
Simple termination	+	-	-	+	-	+
Wide common-mode range	-	+	+	+	-	-
Process independent	+	-	+	+	+	+
Allows integration w/digital	+	-	-	-	+	+
Cable breakage/splicing issues	+	+	-	+	+	+
Long distance transmission	-	+	+	+	-	-
Industrial temp/voltage range	+	+	+	+	+	+

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2.2.0 LVDS DRIVERS & RECEIVERS

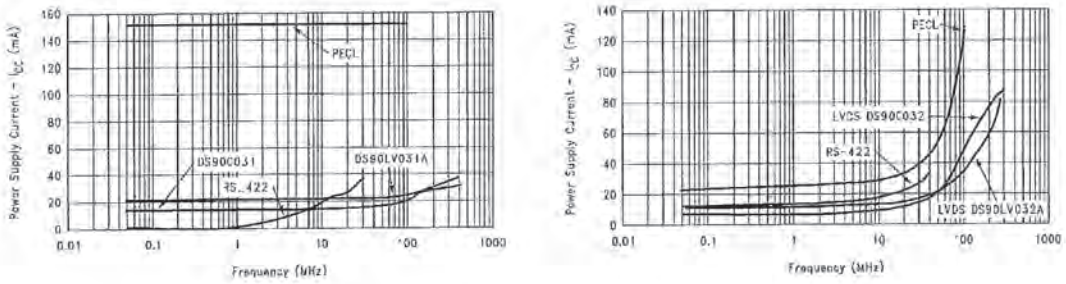
The most basic LVDS devices are the driver and receiver. These translate TTL to LVDS and back to TTL.

LVDS Drivers and Receivers Convert TTL to LVDS and Back to TTL.

Drivers and receivers transmit high-speed data across distances up to 10m with very low power, noise and cost.

Parameter	LVDS	PECL	Optics	RS-422	GTL	TTL
Output voltage swing	±350mV	±800mV	n/a	±2V	1.2V	2.4V
Receiver threshold	±100mV	±200mV	n/a	±200mV	100mV	1.2V
Speed (Mbps)	>400	>400	>1000	<30	<200	<100
Dynamic power	Low	High	Low	Low	High	High
Noise	Low	Low	Low	Low	Med	High
Cost	Low	High	High	Low	Low	Low

The table above summarizes that only LVDS can deliver the high-speed, ultra-low power, and low cost without compromise. PECL and ECL are expensive and consume too much power. TTL/CMOS is cheap, but is noisy and burns a lot of power at high-speeds. Fiber optics are expensive and have cables and connectors which are hard to manage.



I_{CC} vs. Frequency for 5V DS90C031/032 LVDS, 41LG/LF PECL, and 26C31/32 RS-422 Devices.

2.2.1 100Mbps Serial Interconnect

LVDS drivers and receivers are generally used to create serial or pseudo-serial point-to-point interconnects from 1Mbps to >400Mbps per channel. The following example summarizes the total performance and cost advantages of using LVDS over PECL or TTL for a serial 100Mbps 1 meter point-to-point link. Significantly higher data rates can be achieved for LVDS and PECL.

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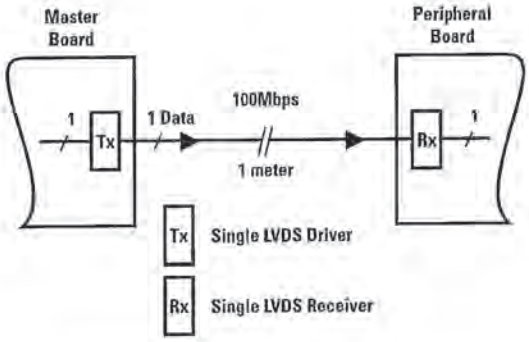

100Mbps Board-to-Board Link

100Mbps Serial Bitstream

Performance Estimate				
Characteristic	**Parameter**	**LVDS**	**TTL**	**PECL**
Speed	Application Data Rate (Mbps)	100	100	100
	Max Capability per Channel (Mbps)	400	100	400
Power Consumption	Dynamic (mA) (@ 50MHz)	Low	High	Medium
	Static (mA)	8	10	48
Noise	Low EMI	+++	---	++
	Low Bounce	+++	---	++
Relative System Cost	**Total**	**4.05**	**3.30**	**6.10**
Cost Estimate				
Subsystem	**Parameter**	**LVDS**	**TTL**	**PECL**
General	Single-Ended or Differential	Differential	Single-Ended	Differential
	TTL Bus Width	1	1	1
	TTL Bus Speed (MHz)	50	50	50
	# Master Boards	1	1	1
	# Slave Boards	1	1	1
Transceivers	Description	DS90LV017A/018A	74LVT125	10ELT20/21
	# Drivers/Board (Master Board)	1	1	1
	# Rec/Board (Peripheral Board)	1	1	1
	Unit Cost	0.70	0.55	2.00
	Silicon Cost per Board	1.40	1.10	4.00
Termination	Voltage	None	None	None
	# Termination Regulators	0	0	0
	Unit Cost	0.00	0.00	0
	# Termination Resistors	1	2	2
	Unit Cost	0.05	0.05	0.05
	# Termination Capacitors	0	0	0
	Unit Cost	0.00	0.00	0.00
	Total Termination Cost	0.05	0.10	0.10
Transmission Medium	Cable Type	2 Pair CAT3	2 Pair CAT3	2 Pair CAT3
	Distance	1m	1m	1m
	#Conductors	2	2	2
	#Cables	1	1	1
	Connector Type	4-pin Wire to Board	4-pin Wire to Board	4-pin Wire to Board
	Unit Cable+Connector Assembly Cost	2.00	2.00	2.00
	Total Media Cost	2.00	2.00	2.00
Total Relative System Cost		**3.45**	**3.20**	**6.10**

Performance and Cost Estimates

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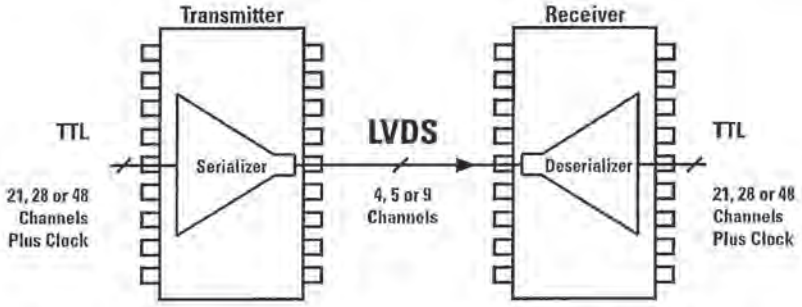
The preceding example shows that LVDS provides a high-speed link with minimal noise, power, and cost. LVDS also creates an easy migration path to higher speeds, lower supply voltages, and higher integration that the other do not.

2.3.0 LVDS CHANNEL LINK SERIALIZERS

The speed of the LVDS line drivers and receivers is limited by how fast the TTL signals can be switched. Therefore, National has introduced a family of Channel Link serializers and deserializers. Instead of using one LVDS channel for every TTL channel, the Channel Link devices send multiple TTL channels through every LVDS channel thereby matching the speed of LVDS to that of TTL.



National's Channel Link Serializers/Deserializers can Dramatically Reduce the Size (and Cost) of Cables and Connectors.

Using fewer channels to convey data also means power and noise can be lower. The biggest advantage, however, is the significant reduction of cable and connector size. Since cables and connectors are usually quite expensive compared to silicon, dramatic cost savings can be achieved. Channel Link chipsets reduce cable size by up to 80%, reducing cable costs by as much as 50%. Plus, smaller cables are more flexible and user-friendly.

LVDS Channel Link serializer/deserializer devices take the inherent high-speed low power, noise, and cost advantages of LVDS and capitalize on the slow speed of TTL to generate significant benefits. For a small increase in silicon cost, Channel Link products can dramatically reduce total system costs and improve total system performance. Therefore, the total system should be evaluated if the true advantages are to be quantified. The following sections summarizes the cost and performance benefits of using Channel Link devices.

2.2.1 1Gbps 16-bit Interconnect

National's Channel Link serializers/deserializers take the benefits of LVDS (high-speed and low power, noise, and cost) and add serialization to further reduce cable, connector, and PCB size and cost. Channel Link is a great solution for high-speed data bus extension when the overhead of protocols is not desired. The following example compares the total performance and cost of moving a 16-bit 66MHz bus across 1 meter of cable using the 3V 66MHz 21-bit DS90CR215/216 Channel Link devices versus other solutions. Driving TTL signals over 1 meter of distance may be very risky due to the limited tolerance to noise (<400mV) and also transmission line problems generated by the TTL driver.

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16-Bit Cable Interconnect

Performance Estimate

Characteristic	Parameter	Channel Link	TTL	GTL	ECL	Fibre Channel
Speed	Application Data Rate (Mbps)	1056	1056	1056	1056	1056
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 66MHz)	180	300	500	300	?
	Static (mA) (Outputs Disabled)	0.02 (Power Dn)	1	50	50	135
Noise	Low EMI	+++	- - -	- -	+	+++
	Low Bounce	+++	- - -	- -	++	+++
Ergonomics	Compact System Size	+++	- -	- -	- - -	+++
	Compact Transmission Medium Size	+++	-	+	+	+++
	Low Weight	+++	-	-	-	+++
Relative System Cost	Total	25.50	55.80	58.80	71.80	77.60

Cost Estimate

Subsystem	Parameter	Channel Link	TTL	GTL	ECL	Fibre Channel
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Differential	Differential ECL
	TTL Bus Width	16	16	16	16	16
	TTL Bus Speed (MHz)	66	66	66	66	66
	Multiplexed Scheme?	Yes	No	No	No	Yes
	# Master Boards	1	1	1	1	1
	# Slave Boards	1	1	1	1	1
Transceivers	Description	3V 21:4 Channel Link	ALVT 16-Bit	GTL 18-Bit	9-Bit Translators	Fibre Channel
	# Drivers/Board (Master Board)	1	1	1	2	1
	# Rec/Board (Peripheral Board)	1	1	1	2	1
	Unit Cost	3.70	2.40	3.25	5.00	20.00
	Silicon Cost per Board	7.40	4.80	6.50	20.00	40.00
PC Board	Layers	4	12	12	12	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	15.00	15.00	15.00	15.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	# Termination Regulators	0	0	1	1	1
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	# Termination Resistors	10	16	16	16	32
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	# Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	0.80	1.80	1.80	2.60
Transmission Medium	Cable Type	SCSI2 CAT3 Cable	Shielded Flat Cable	Shielded Flat Cable	SCSI2 CAT3 Cable	CAT5 Cable
	Distance	2m	2m	2m	2m	2m
	#Data+Clock Conductors	8	17	17	34	2
	#Power+Ground Conductors	4	10	10	15	2
	#Cables	1	1	1	1	1
	Connector Type	0.050 D - 20	D - 37	D - 37	0.050 D - 50	DB-9
	Unit Cable+Connector Assembly Cost	20.00	30.00	30.00	30.00	15.00
	Total Media Cost	15.00	30.00	30.00	30.00	15.00
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.3	1.2	1.2	1.2
	Total Add'l Power Supply Cost	0.00	5.00	5.00	5.00	5.00
Total Relative System Cost		22.90	55.60	58.30	71.80	77.60

Performance and Cost Estimates

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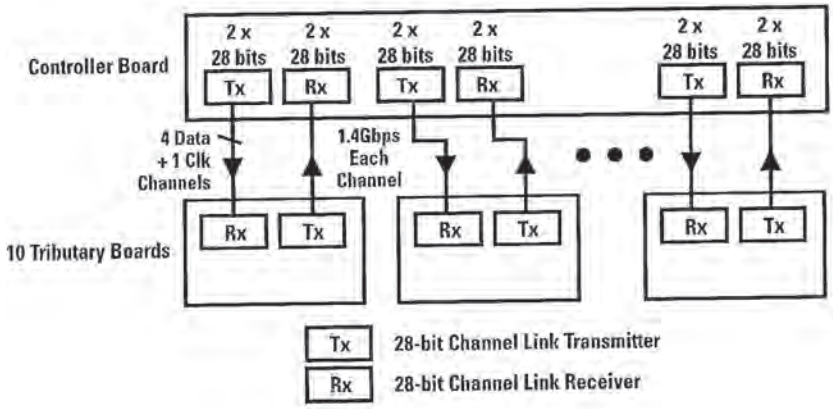
2.2.2 1.4Gbps 56-Bit Backplane

In some large datacom and telecom systems, it is necessary to construct a very large, high-speed backplane. There is generally an inverse relationship between the size of a backplane and its maximum speed. In other words, if you try to make a backplane too large, the heavy loading will severely hamper backplane speed and make power and noise a big problem. Therefore, connecting or extending smaller backplanes via a high-speed cable interconnect is often the only solution. The previous examples illustrates how Channel Link may be used to accomplish this over cable. The cost benefits of using Channel Link to shrink cable and connector costs are clear. What would happen, however, if Channel Link were used to form or extend a backplane using a PCB as the medium. The following examples shows how Channel Link can reduce the size and number of layers of the printed circuit board transmission medium in the same way as Channel Link reduces the size and cost of cables.



1.4Gbps Backplane Using Point-to-Point Channel Links

56-Bit Backplane

Performance Estimate						
Characteristic	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
Speed	Application Data Rate (Mbps)	1400	1400	1400	1400	1400
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 50MHz)	2600	10000	6000	16000	?
(Loaded Tx/Rx's only)	Static (mA)	0.4 (Power on)	40	1840	3402	3818
Noise	Low EMI	+++	---	+	+	++
	Low Bounce	+++	---	+	+	++
Ergonomics	Compact System Size	++	+	+	+	++
	Compact Transmission Medium Size	++	-	+	+	++
	Fans?	No	No	No	Yes	Yes
	Low Weight	+++	-	-	-	+++
Relative System	Cost Per Board	51.05	66.12	75.04	191.04	574.22
	Total	510.50	661.20	750.40	1910.40	5742.20

Performance Estimate

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Cost Estimate						
Subsystem	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Single-Ended	Differential
	TTL Bus Width	56	56	56	56	56
	TTL Bus Speed (MHz)	50	50	50	50	50
	Multiplexed Scheme?	Yes	No	No	No	Yes
	Number Tributary Boards	10	10	10	10	10
	Number Channels in Link	10	56	56	56	14
	Number Conductors (Data)	20	56	56	56	28
	Number Conductors (CLK)	1	1	1	1	1
Transceivers	Description	28:5 Channel Link	LVT 16-Bit	GTL 18-Bit	9-Bit	Fibre Channel
	# Transceivers/Board (Trib Board)	4	4	4	14	14
	# Transceivers/Board (Ctrlr Board)	4	4	4	14	14
	Unit Cost	3.70	2.40	3.25	5.00	20.00
	Silicon Cost per Board	29.60	19.20	26.00	140.00	560.00
PC Board	Layers	12	26	26	26	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	100.00	100.00	150.00	50.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	Number Termination Regulators	0	0	14	14	14
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	Number Termination Resistors	10	224	128	128	14
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	Number Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	11.20	20.40	20.40	14.70
Transmission Medium	Type	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane
	Distance	<1m	<1m	<1m	<1m	<1m
	Layers	12	26	26	26	12
	Size (Normalized)	1	1	1	1	1
	Number Media	1	1	1	1	1
	Additional Media Cost	0.00	200.00	200.00	200.00	0.00
	Total Add'l Trans. Media Cost	0.00	200.00	200.00	200.00	0.00
Connectors	Connector Type	Header	VME	VME	VME	Header
	Number Pins (Data+ CLK)	21	57	57	57	29
	Number Pins (Power/GND)	5	38	38	7	7
	Total Connector Pins	26	96	96	64	36
	Number Connector Pairs	1	1	1	1	1
	Cost of Pair	3.00	10.00	10.00	8.00	3.75
	Connector Cost per Board	3.00	10.00	10.00	8.00	3.75
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.5	1.5	1.7	1.4
	Total Add'l Power Supply Cost	0.00	50.00	50.00	60.00	40.00
Total Relative System Cost Per Board		49.21	66.64	74.84	191.04	574.22
Total Relative System Cost		492.10	666.40	748.40	1910.40	5742.20

Cost Estimate

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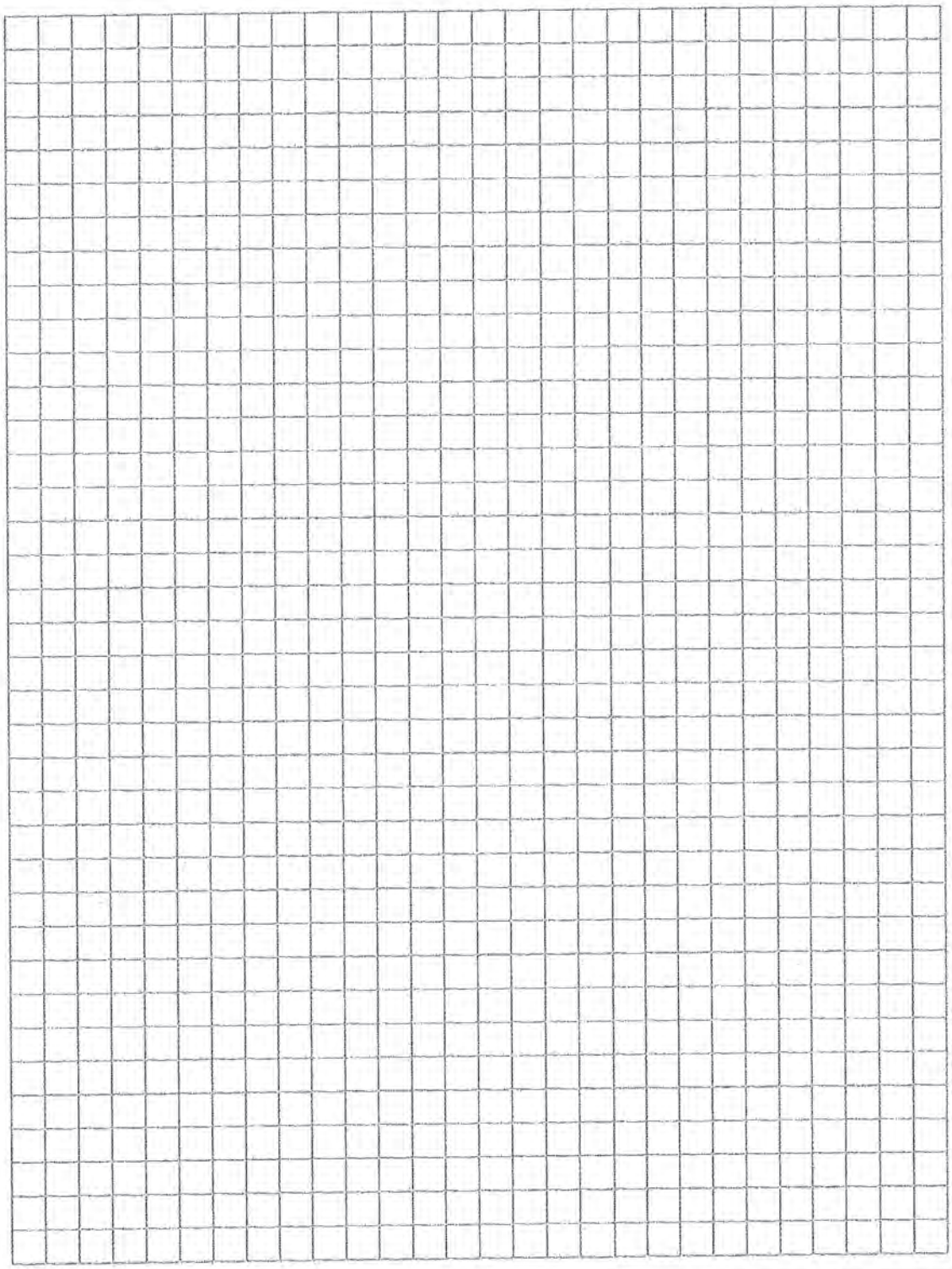
NOTES



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Selecting an LVDS Device/ LVDS Families

Chapter 3

3.0.0 SELECTING AN LVDS DEVICE

3.1.0 GENERAL

National is continually expanding its portfolio of LVDS devices. The devices listed below are current at the time this book goes to press. For the latest list of LVDS devices, please visit our LVDS website at: www.national.com/appinfo/lvds/

On this site, you will find the latest LVDS datasheets, application notes, selection tables, FAQs, modeling information/files, white papers, LVDS News, and much much more! The Web is constantly updated with new documents as they are available.

Application questions should be directed to your local National Semiconductor representative or to the US National Interface Hotline: 1-408-721-8500 (8 a.m. to 5 p.m. PST).

LVDS products are classified by device types. Please see below for a short description of each device type and selection table that was current at the time this edition of the LVDS Owner's Manual was printed. Again, visit our web site for the latest information.

3.1.1 Do I need LVDS?

If Megabits or Gigabits @ milliwatts are needed, then LVDS may be the answer for you! It provides high-speed data transmission, consumes little power, rejects noise, and is robust. It is ideal for interconnects of a few inches to tens of meters in length. It provides an ideal interface for chip-to-chip, card-to-card, shelf-to-shelf, rack-to-rack or box-to-box communication.

3.1.2 Which part should I use?

If point-to-point or multidrop configuration is needed – see the LVDS Line Driver/Receivers or Channel Link Family.

If multipoint or certain multidrop configurations are needed – then Bus LVDS offers the technology best suited for these applications.

Parallel? Serialize? Or Serial? – depends upon the application. Small busses typically use the simple PHY parts. However, if the bus is wide, then serialization may make the most sense. Serialization provides a smaller interconnect and reduces cable and connector size and cost. For this application, refer to the Channel Link and also the Bus LVDS SER/DES parts.

3.2.0 LVDS LINE DRIVERS & RECEIVERS

LVDS line drivers and receivers are used to convey information over PCB trace or cable if;

1. You only have a few channels of information to transmit, or
2. Your data is already serialized.

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The following table summarizes National's LVDS line drivers and receivers. These devices are also referred to as simple PHYs.

LVDS Driver/Receiver/Transceiver Products

Order Number	# Dr.	# Rec.	Sup. Volt.	Temp	Speed per Channel	Typ I_{CC}@ 1Mbps (mA)	Max I_{CC} Disabled (mA)	Driver Max tpd (ns)	Driver Max Ch Skew (ns)	Receiver Max tpd (ns)	Receiver Max Ch Skew (ns)	Package	Comments
DS90LV047ATM	4	0	3.3	Ind	>400Mbps	20	6	1.7	0.5	—	—	16SOIC	
DS90LV047ATMTC	4	0	3.3	Ind	>400Mbps	20	6	1.7	0.5	—	—	16TSSOP	
DS90LV048ATM	0	4	3.3	Ind	>400Mbps	9	5	—	—	2.7	0.5	16SOIC	
DS90LV048ATMTC	0	4	3.3	Ind	>400Mbps	9	5	—	—	2.7	0.5	16TSSOP	
DS90LV031ATM	4	0	3.3	Ind	>400Mbps	21	6	2.0	0.5	—	—	16SOIC	
DS90LV031ATMTC	4	0	3.3	Ind	>400Mbps	21	6	2.0	0.5	—	—	16TSSOP	
DS90LV032ATM	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.3	0.5	16SOIC	
DS90LV032ATMTC	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.3	0.5	16TSSOP	
DS90LV031BTM	4	0	3.3	Ind	>400Mbps	22	6	2.0	0.5	—	—	16SOIC	Available soon
DS90LV031BTMTC	4	0	3.3	Ind	>400Mbps	22	6	2.0	0.5	—	—	16TSSOP	Available soon
DS90LV032BTM	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.0	0.5	16SOIC	Available soon
DS90LV017ATM	1	0	3.3	Ind	>600Mbps	7	—	1.5	—	—	—	8 SOIC	
DS90LV017M	1	0	3.3	Com	>155Mbps	5.5	—	6.0	—	—	—	8 SOIC	
DS90LV018ATM	0	1	3.3	Ind	>400Mbps	5.5	—	—	—	2.5	—	8 SOIC	
DS90LV019TM	1	1	3.3/5	Ind	>100Mbps	16/19	7/8.5	7.0/6.0	—	9.0/8.0	—	14 SOIC	
DS90LV027ATM	2	0	3.3	Ind	>600Mbps	14	—	1.5	0.8	—	—	8 SOIC	
DS90LV027M	2	0	3.3	Com	>155Mbps	9	—	6.0	—	—	—	8 SOIC	
DS90LV028ATM	0	2	3.3	Ind	>400Mbps	5.5	—	—	—	2.5	0.5	8 SOIC	
DS90LV031AW-QML	4	0	3.3	Mil	>400Mbps	21	12	3.6	1.75	—	—	16CERPAK	Mil spec
DS90C031TM	4	0	5	Ind	>155Mbps	15.5	4	3.5	1.0	—	—	16SOIC	
DS90C032TM	0	4	5	Ind	>155Mbps	5	10	—	—	6.0	1.5	16 SOIC	
DS90C031BTM	4	0	5	Ind	>155Mbps	15.5	4	3.5	1.0	—	—	16 SOIC	Pwr Off Hi-Z
DS90C032BTM	0	4	5	Ind	>155Mbps	5	10	—	—	6.0	1.5	16 SOIC	Pwr Off Hi-Z
DS90C031E-QML	4	0	5	Mil	>100Mbps	15.5	10	5.0	3.0	—	—	20 LCC	Military-883
DS90C032E-QML	0	4	5	Mil	>100Mbps	5	11	—	—	8.0	3.0	20 LCC	Military-883
DS90C031W-QML	4	0	5	Mil	>100Mbps	15.5	10	5.0	3.0	—	—	16Flatpack	Military-883
DS90C032W-QML	0	4	5	Mil	>100Mbps	5	11	—	—	8.0	3.0	16Flatpack	Military-883
DS90C401M	2	0	5	Ind	>155Mbps	4	—	3.5	1.0	—	—	8 SOIC	
DS90C402M	0	2	5	Ind	>155Mbps	4.5	—	—	—	6.0	1.5	8 SOIC	
DS36C200M	2	2	5	Com	>100Mbps	12	10	5.5	—	9.0	—	14 SOIC	1394 Link

Note: Evaluation boards utilize a quad driver/receiver pair to perform generic cable/PCB/etc LVDS driver/receiver evaluations, order number LVDS47/48EVK.

3.3.0 LVDS DIGITAL CROSSPOINT SWITCHES

For routing of high-speed point-to-point busses, crosspoint switches may be used. They are also very useful in applications with redundant backup interconnects for fault tolerance. This first device in this planned family of products is now available. It is a 2x2 Crosspoint that operates above 800Mbps and generates extremely low jitter.

LVDS Digital Crosspoint Switches

Order Number	Description	Supply Voltage	Speed	Number of Inputs	Number of Outputs	Package
DS90CP22M-8	2 x 2 800Mbps LVDS Crosspoint Switch	3.3V	800Mbps	2	2	16SOIC

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3.4.0 LVDS CHANNEL LINK SERIALIZERS/DESERIALIZERS

If you have a wide TTL bus that you wish to transmit, use one of National's Channel Link devices. Channel Link will serialize your data for you, saving you money on cables and connectors and helping you avoid complex skew problems associated with a completely parallel solution. The following table summarizes National's Channel Link devices.

LVDS Channel Link Serializer/Deserializer Products

Order Number	Mux/Demux Ratio	Type	Supply Voltage	Clock Frequency	Max Throughput	Package	Comments	Eval Board Order Number
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	48TSSOP		CLINK5V28BT-66
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	48TSSOP		CLINK5V28BT-66
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	48TSSOP		CLINK5V28BT-66
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	48TSSOP		CLINK5V28BT-66
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	48TSSOP		CLINK3V28BT-66
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP		CLINK3V28BT-66
DS90CR216AMTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP	Enhanced Set/Hold Times	CLINK3V28BT-66
DS90CR217MTD	21:3	Transmitter	3.3	20-85MHz	1.78Gbps	48TSSOP		See Note
DS90CR218AMTD	21:3	Receiver	3.3	20-85MHz	1.78Gbps	48TSSOP		See Note
DS90CR218MTD	21:3	Receiver	3.3	20-75MHz	1.575Gbps	48TSSOP		See Note
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	56TSSOP		CLINK5V28BT-66
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	56TSSOP		CLINK5V28BT-66
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	56TSSOP		CLINK5V28BT-66
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	56TSSOP		CLINK5V28BT-66
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	56TSSOP		CLINK3V28BT-66
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP		CLINK3V28BT-66
DS90CR286AMTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP	Enhanced Set/Hold Times	CLINK3V28BT-66
DS90CR287MTD	28:4	Transmitter	3.3	20-85MHz	2.38Gbps	56TSSOP		See Note
DS90CR288MTD	28:4	Receiver	3.3	20-75MHz	2.10Gbps	56TSSOP		See Note
DS90CR288AMTD	28:4	Receiver	3.3	20-85MHz	2.38Gbps	56TSSOP		See Note
DS90CR483VJD	48:8	Transmitter	3.3	32.5-112MHz	5.37Gbps	100TQFP		CLINK3V48BT-112
DS90CR484VJD	48:8	Receiver	3.3	32.5-112MHz	5.37Gbps	100TQFP		CLINK3V48BT-112

Note: 85MHz eval boards will be available in the future. For immediate needs, use CLINK3V28BT-66 with 75 or 85MHz parts.

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3.5.0 LVDS FPD-LINK

Use National's FPD Link to convey graphics data from your PC or notebook motherboard to your flat panel displays. The next table summarizes National's FPD Link devices. This family has been extended with the LVDS Display Interface chipset that provides higher resolution support and long cable drive enhancements. The LDI Chipset is ideal for desktop monitor applications and also industrial display applications. The FPD-Link receiver function is also integrated into the timing controller devices to provide a small single-chip solution for TFT Panels.

LVDS Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI)

Order Number	Color Bits	Type	Supply Voltage	Max Clock Frequency	Clock Edge Strobe	Package	Comments	Eval Board Order Number
DS90CF561MTD	18-bit	Transmitter	5	40MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR561MTD	18-bit	Transmitter	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF562MTD	18-bit	Receiver	5	40MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR562MTD	18-bit	Receiver	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CR581MTD	24-bit	Transmitter	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65
DS90CF563MTD	18-bit	Transmitter	5	65MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR563MTD	18-bit	Transmitter	5	65MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF564MTD	18-bit	Receiver	5	65MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR564MTD	18-bit	Receiver	5	65MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF583MTD	24-bit	Transmitter	5	65MHz	Falling	56TSSOP		FLINK5V8BT-65
DS90CR583MTD	24-bit	Transmitter	5	65MHz	Rising	56TSSOP		FLINK5V8BT-65
DS90CF584MTD	24-bit	Receiver	5	65MHz	Falling	56TSSOP		FLINK5V8BT-65
DS90CR584MTD	24-bit	Receiver	5	65MHz	Rising	56TSSOP		FLINK5V8BT-65
DS90C363AMTD	18-bit	Transmitter	3.3	65MHz	Programmable	48TSSOP		FLINK3V8BT-65 *
DS90CF363AMTD	18-bit	Transmitter	3.3	65MHz	Falling	48TSSOP		FLINK3V8BT-65 *
DS90CF364MTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP		FLINK3V8BT-65 *
DS90CF364AMTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP	50% CLKOUT	FLINK3V8BT-65 *
DS90C383AMTD	24-bit	Transmitter	3.3	65MHz	Programmable	56TSSOP		FLINK3V8BT-65
DS90CF383AMTD	24-bit	Transmitter	3.3	65MHz	Falling	56TSSOP		FLINK3V8BT-65
DS90CF384MTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP		FLINK3V8BT-65
DS90CF384AMTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP	50% CLKOUT	FLINK3V8BT-65
DS90C365MTD	18-bit	Transmitter	3.3	85MHz	Programmable	48TSSOP		See Note *
DS90CF366MTD	18-bit	Receiver	3.3	85MHz	Falling	48TSSOP		See Note *
DS90C385MTD	24-bit	Transmitter	3.3	85MHz	Programmable	56TSSOP		See Note
DS90CF386MTD	24-bit	Receiver	3.3	85MHz	Falling	56TSSOP		See Note
DS90C387VJD	48-bit	Transmitter	3.3	112MHz	Programmable	100TQFP		LDI3V8BT-112
DS90C387AVJD	48-bit	Transmitter	3.3	112MHz	Programmable	100TQFP	Non-DC Balanced	NA
DS90CF388VJD	48-bit	Receiver	3.3	112MHz	Falling	100TQFP		LDI3V8BT-112
DS90CF388AVJD	48-bit	Receiver	3.3	112MHz	Falling	100TQFP	Non-DC Balanced	NA

* For 18-bit evaluation, use 24-bit board for evaluation purposes.
Note: 85MHz eval boards will be available in the future. For immediate needs, FLINK3V8BT-65 can be used with 85MHz part.

LVDS Flat Panel Display Timing Controller Products

Order Number	Color Bits	Resolutions Supported	Supply Voltage	Max Clock Frequency	TCON Core	Package	Input/Output	Eval Board Order Number
FPD85310VJD	6 or 8	XGA/SVGA	3.3	65MHz	Programmable	TQFP	LVDS input/TTL dual port output	Call
FPD87310VJD	6 or 8	XGA/SVGA	3.3	65MHz	Programmable	TQFP	LVDS input/RSDS single port output	Call

Note: FPD8710 in sampling phase.

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3.6.0 BUS LVDS

Bus LVDS is an extension of the LVDS line drivers and receivers family. They are specifically designed for multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30 to 50Ω range. Bus LVDS drivers provide about 10mA of output current so that they provide LVDS swings with heavier termination loads. Transceivers and Repeaters are currently available in this product family. A "10-bit" Serializer and Deserializer family of devices is also available that embeds and recovers the clock from a single serial stream. This chipset also provides a high level of integration reducing complexity and overhead to link layer ASICs. Clock recovery and "Random Lock" digital blocks are integrated with the core interface line driving and receiving functions. The Deserializer (DS92LV1212/1224) can also be hot-plugged into a live data bus and does not require PLL training.

Special functions are also being developed using BLVDS/LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs (DS92CK16) and a Repeater/MUX with selectable drive levels (DS92LV222A) are available.

Bus LVDS Products

Order Number	Description	Supply Voltage	Speed	Features	Package
DS92LV010ATM	Single Bus LVDS Transceiver	3.3/5	155Mbps/Ch	3.3V or 5V Operation	8SOIC
DS92LV222ATM	Bus LVDS or LVDS Repeater/Mux	3.3	200Mbps/Ch	Repeater, Mux, or 1:2 Clock Driver Modes	16SOIC
DS92LV090ATVEH	9-Chennel Bus LVDS Transceiver	3.3	200Mbps/Ch	Low Part-to-Part Skew	64PQFP
DS92LV1021TMSA	10:1 Serializer w/Embedded Clock	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1210TMSA	1:10 Deserializer w/Clock Recovery	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1212TMSA	1:10 Random Lock Deserializer w/Clk Recovery	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1023TMSA	10:1 Serializer w/Embedded Clock	3.3	66MHz	660Mbps Data Payload Over Single Pair	28SSOP
DS92LV1224TMSA	1:10 Random Lock Deserializer w/Clk Recovery	3.3	66MHz	660Mbps Data Payload Over Single Pair	28SSOP
DS92CK16TMTC	1:6 Clock Distribution	3.3	125MHz	50ps TTL output channel-to-channal skew	24TSSOP
More to come...					

3.7.0 SUMMARY

Over 75 different LVDS products are currently offered by National. For the latest in product information, and news, please visit National's LVDS web site at: www.national.com/appinfo/lvds/

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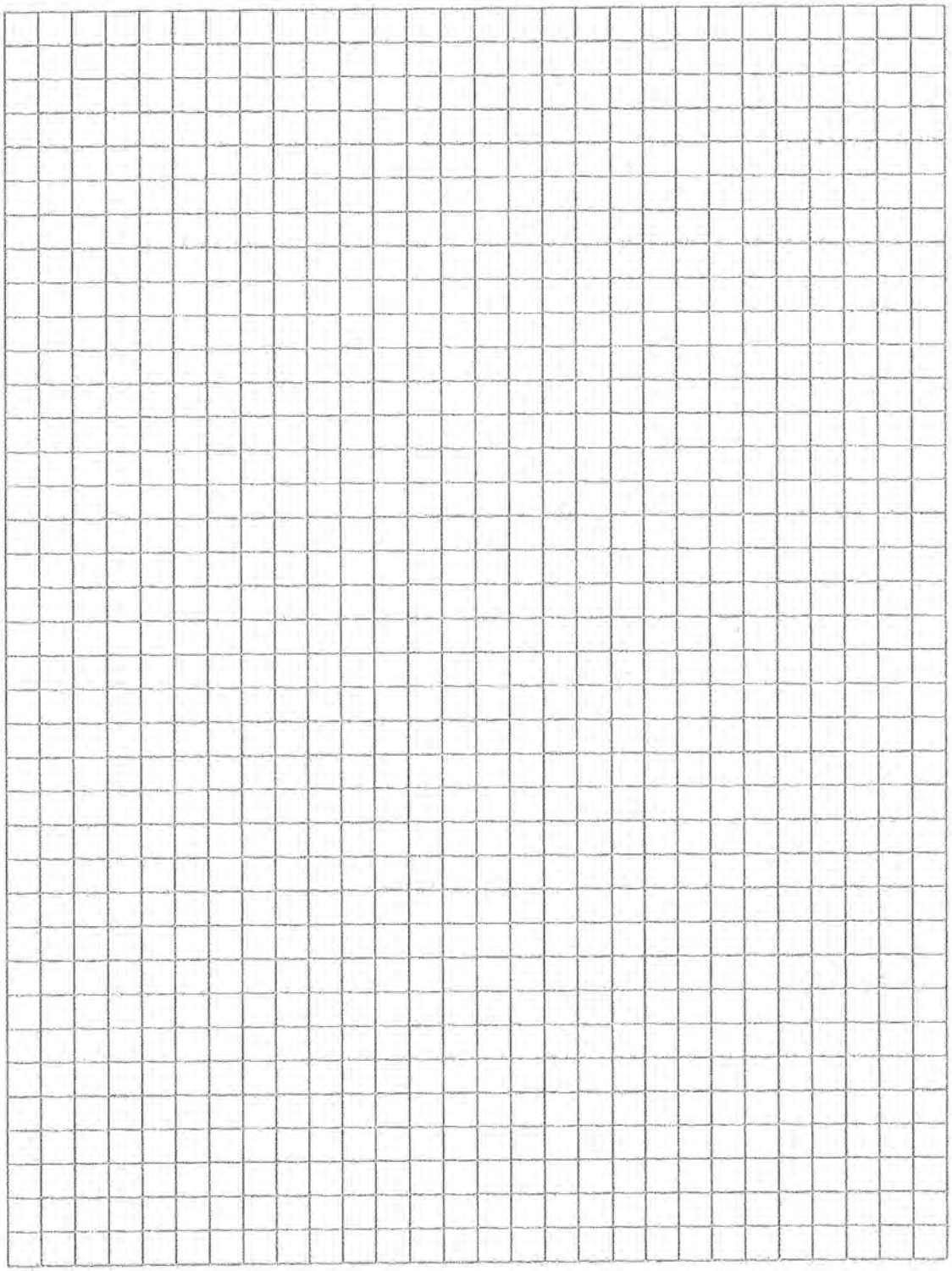
NOTES



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Designing with LVDS

Chapter 4

4.0.0 DESIGNING WITH LVDS

4.1.0 PCB BOARD LAYOUT TIPS

Now that we have explained how LVDS has super speed, and very low: power, noise, and cost, many people might assume that switching to LVDS (or any differential technology) will solve all of their noise problems. It will not, but it can help a lot! LVDS has low swing, differential, ~3.5mA current-mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond which means that every interconnect will act as a transmission line except the very shortest. Therefore, knowledge of ultra-high-speed board design and differential signal theory is required. Designing high-speed differential boards is not difficult or expensive, so familiarize yourself with these techniques before you begin your design.

Generalized Design Recommendations are provided next.

The edge rate of an LVDS driver means that impedance matching is very important even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI. You should use controlled differential impedance traces as soon as you can after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12mm (0.5in). Also, avoid 90° turns since this causes impedance discontinuities; use 45 turns, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs which looks like and radiates as common-mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias to minimize inductance to the power planes.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are inexpensive and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should provide maximum performance and be quick and easy to develop.

4.1.1 PC Board

a) Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals. Dedicating planes for V_{CC} and Ground are typically required for high-speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground can also create an excellent high frequency bypass capacitance.

b) Isolate fast edge rate CMOS/TTL signals from LVDS signals, otherwise the noisy single-ended CMOS/TTL signals may couple crosstalk onto the LVDS lines. It is best to put TTL and LVDS signals on a different layer(s) which should be isolated by the power and ground planes.

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c) Keep drivers and receivers as close to the (LVDS port side) connectors as possible. This helps to ensure that noise from the board is not picked up onto the differential lines and escapes the board as EMI from the cable interconnect. This recommendation also helps to minimize skew between the lines. Skew tends to proportional to length, therefore by limiting length also limits skew.

d) Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power Supply: A 4.7µF or 10µF 35V tantalum capacitor works well between supply and ground. Choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 to 300MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} Pins: One or two multi-layer ceramic (MLC) surface mount capacitors (0.1µF and 0.01µF) in parallel should be used between each V_{CC} pin and ground if possible. For best results, the capacitors should be placed as close as possible to the V_{CC} pins to minimize parasitic effects that defeat the frequency response of the capacitance. Wide (>4-bits) and PLL-equipped (e.g. Channel Link & FPD-Link) LVDS devices should have at least two capacitors per power type, while other LVDS devices are usually fine with a 0.1µF capacitor. The bottom line is to use good bypassing practices. EMI problems many times start with power and ground distribution problems. EMI can be greatly reduced by keeping power and ground planes quiet.

e) Power and ground should use wide (low impedance) traces. Do not use 50Ω design rules on power and ground traces. Their job is to be a low impedance point.

f) Keep ground PCB return paths short and wide. Provide a return path that create the smallest loop for the image currents to return.

g) Cables should employ a ground return wire connecting the grounds of the two systems. This provides for common-mode currents to return on a short known path. See Chapter 5, Section 5.3.0

h) Use two vias to connect to power and ground from bypass capacitor pads to minimize inductance effects. Surface mount capacitors are good as they are compact and can be located close to device pins.

4.1.2 Traces

a) Edge-coupled Microstrip, Edge-coupled Stripline, or Broad-side Striplines all work well for differential lines.

b) Traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance. See section 4.1.3.

c) Edge-coupled Microstrip line offer the advantage that a higher differential Z_O is possible (100 to 150Ω). Also it may be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

d) Stripline may be either edge-couple or broad-side lines. Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also coupling of noise onto the lines. They also require the use of via to connect to them.

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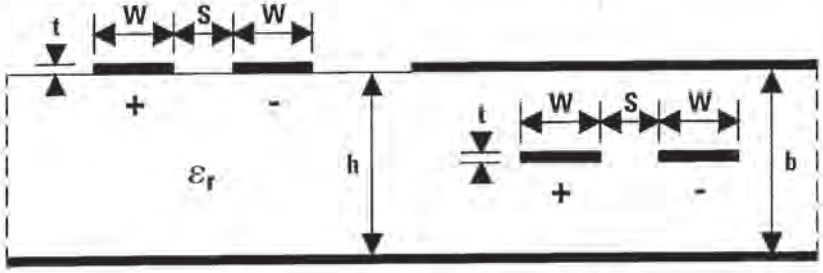
4.1.3 Differential Traces

a) Use controlled impedance PCB traces which match the differential impedance of your transmission medium (i.e. cable) and termination resistor. Route the differential pair traces as close together as possible as soon as they leave the IC. This helps to eliminate reflections and ensures that noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.



When designing for a specific differential Z_O (Z_{DIFF}) for edge-coupled lines, it is recommended that you adjust trace width "W" to alter Z_{DIFF}. It is recommended to not adjust "S" which should be the minimum spacing specified by your PCB vendor for line-to-line spacing. You can use National's Transmission Line RAPIDESIGNER slide rule (LIT# 633200-001 metric or LIT# 633201-001 English units) and application note AN-905, LIT# 100905-002) to calculate Z_O and Z_{DIFF}, or you can use the equations below for edge-coupled differential lines:

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.48e^{-0.96\frac{S}{h}}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.374e^{-2.9\frac{S}{h}}\right) \text{ Ohms} \quad \text{Stripline}$$

$$Z_0 = \frac{60}{\sqrt{0.475\,\varepsilon_r + 0.67}} \ln\left(\frac{4h}{0.67\,(0.8W + t)}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\,\pi\,(0.8W + t)}\right) \text{ Ohms} \quad \text{Stripline}$$

Note: For edge-coupled striplines, the term "0.374" may be replaced with "0.748" for lines which are closely-coupled (S < 12 mils).

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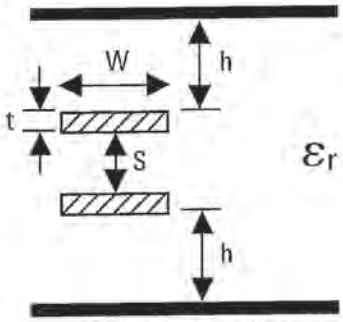
Broadside coupled lines structure can also be used. The dimensions for this type of line are shown below. Broadside coupled striplines can be useful in backplane design as these use only one routing channel and may be easier to route through the connector pin field. An equation with similar accuracy as for the edge-couple lines is:



$$Z_{DIFF} = \frac{80}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(2h+t)}{0.8W+t}\right]\left[1-\frac{h}{4(h+S+t)}\right] \text{ Ohms}$$

Broadside Stripline

Broadside Stripline

Always use consistent dimensions (e.g. all dimensions in mils, centimeters or millimeters) for S, h, W, and t when making calculations.

Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary, please refer to AN-905 for accuracy information and ranges supported.

Common values of dielectric constant (ε_r) for various printed circuit board (PCB) materials is given below. Consult your PCB manufacturer for actual numbers for the specific material that you plan to use. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. GETEK is about 1.5 times as expensive as FR-4, but can be considered for 1000+ MHz designs. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

PCB Material	Dielectric Constant (ε_r)	Loss Tangent
Air	1.0	0
PTFE (Teflon)	2.1-2.5	0.0002-0.002
BT Resin	2.9-3.9	0.003-0.012
Polyimide	2.8-3.5	0.004-0.02
Silica (Quartz)	3.8-4.2	0.0006-0.005
Polyimide/Glass	3.8-4.5	0.003-0.01
Epoxy/Glass (FR-4)	4.1-5.3	0.002-0.02
GETEK	3.8-3.9	0.010-0.015 (1MHz)
ROGERS4350 Core	3.48 ± 0.05	0.004 @ 10G, 23°C
ROGERS4430 Prepreg	3.48 ± 0.05	0.005 @ 10G, 23°C

b) Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, v = c/ε_r where c (the speed of light) = 0.2997mm/ps or 0.0118in/ps). A general rule is to match lengths of the pair to within 100mils.

c) Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to insure isolation between pairs of the differential lines.

d) Minimize the number of via and other discontinuities on the line.

e) Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.

f) Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. Both lines of the pair should be as identical as possible for the best results.

4.1.4 Termination

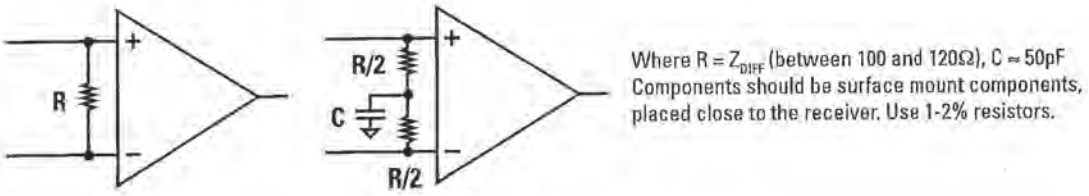
a) Use a termination resistor which best matches the differential impedance of your transmission line. It should be between 90Ω and 130Ω for point-to-point cable applications. Remember that the current-mode outputs need the termination resistor to generate the proper differential voltage. LVDS is not intended to work without a resistor termination.

b) Typically a single resistor across the pair at the receiver end suffices.

c) Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7mm (12mm MAX).

d) Resistor tolerance of 1 or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match the better. Match to the nominal differential impedance of the interconnect.

d) Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This termination is not commonly used or required.



Where R = Z_{DIFF} (between 100 and 120Ω), C ≈ 50pF
Components should be surface mount components, placed close to the receiver. Use 1-2% resistors.

Common Differential Termination Schemes

4.1.5 Unused Pins

LVDS INPUTS - Leave unused LVDS receiver inputs open (floating) for LVDS receiver unless directed differently by the specific component's datasheet. Their internal failsafe feature will lock the outputs high. These unused receiver inputs should not be connected to noise sources like cables or long PCB traces — float them near the pin. LVDS receivers are high-speed, high-gain devices, and only a small amount of noise, if picked up differentially will cause the receiver to respond. This causes false transitions on the output and increased power consumption.

LVDS & TTL OUTPUTS - Leave all unused LVDS and TTL outputs open (floating) to conserve power. Do not tie them to ground.

TTL INPUTS - Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground or in certain cases they may be left open if the datasheet supports this condition. Some devices provide internal pull down (or up) devices to bias the pins. Again, consult the datasheet for information regarding the device's features. This type of information is typically included in the pin description table.

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4.1.6 Probing LVDS Transmission Lines

a) Always use a high impedance (>100kΩ), low capacitance (<0.5pF) probe/scope with a wide bandwidth (>1GHz). Improper probing will give deceiving results. LVDS is not intended to be loaded with a 50Ω load to ground. This will distort the differential and offset voltages of the driver. Differential probes are recommended over two standard scope probes due to match and balance concerns. Bandwidth of the probe/scope combination should be at least 1 or 2GHz. Tektronix and Agilent (HP) both make probes that are well suited for measuring LVDS signals. (See Chapter 7)

4.1.7 Loading LVDS I/O – Preserving Balance

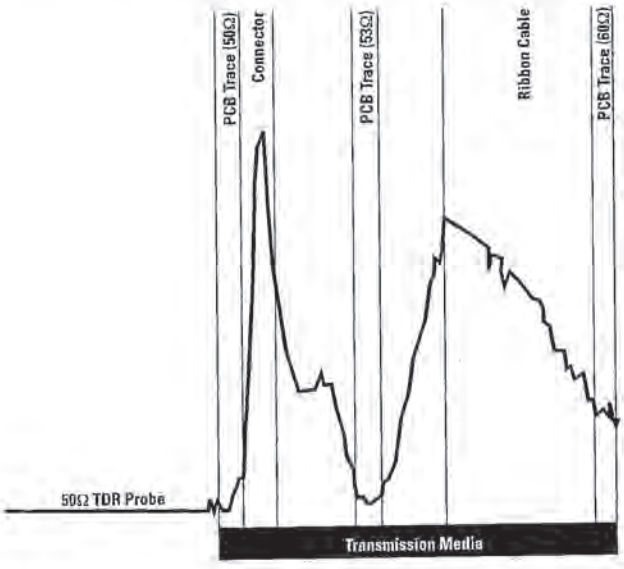
Avoid placing any devices which heavily load the low, ~3.5mA LVDS output drive. If additional ESD protection devices are desired, use components which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

Try not to disturb the differential balance. Treat both members of a pair equally.

4.2.0 RESULTS OF GOOD VS. BAD DESIGN PRACTICES

4.2.1 Impedance Mismatches

It is very common for designers to automatically use any off-the-shelf cables and connectors and 50Ω autorouting when doing new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low swing, current-mode outputs to reduce noise, but that its transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable are not meant for high-speed signals (especially differential signals) and do not always have controlled impedance. The figure below shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedances are neither matched nor controlled. Beware, this example is not worst case — it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.



TDR plot of transmission media with mismatched impedance.

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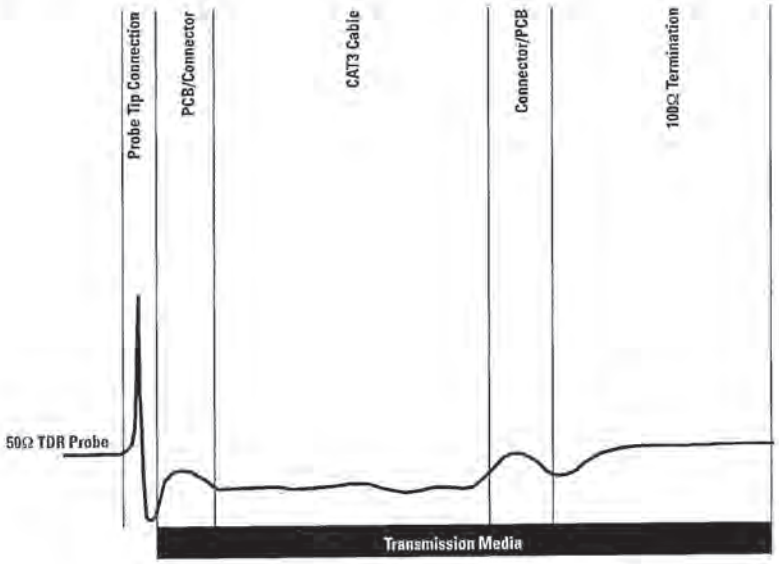
Below is a much improved design which follows most of the high-speed differential design practices listed in Section 4.1.0. The TDR differential impedance plot is much flatter and noise is dramatically reduced.



Minimize impedance variations for best performance.

4.2.2 Crosstalk Between TTL and LVDS Signals

The next two figures show the effects of TTL coupling onto LVDS lines. The first figure shows the LVDS waveforms before coupling, while the second shows the effects of a 25MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 inches. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally — the signal which runs closest to the TTL trace is affected more than the other. This difference will not be rejected by the receiver as common-mode noise and though it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal reducing noise margin. The common-mode noise will be rejected by the receiver, but can radiate as EMI.

LVDS Signals Before Crosstalk

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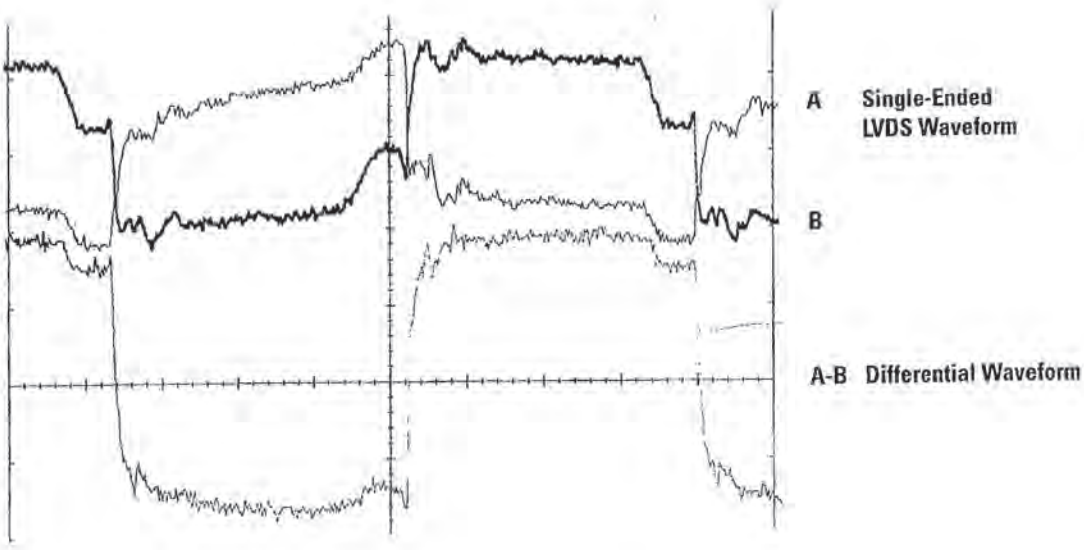

LVDS signals affected by TTL crosstalk.

4.2.3 The "S" Rule

Using the edge-to-edge "S" distance between the traces of a pair, other separations can be defined:

- The distance between two pairs should be >2S.
- The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane.
- If a guard ground trace or ground fill is used, it should be >2S away.

4.3.0 LOWERING ELECTROMAGNETIC INTERFERENCE (EMI)

4.3.1 LVDS and Lower EMI

High-speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1. The low output voltage swing (~350mV)
2. Relatively slow edge rates, dV/dt ~ 0.350V/0.350ns = 1V/ns
3. Differential (odd mode operation) so magnetic fields tend to cancel
4. "Soft" output corner transitions
5. Minimum I_{CC} spikes due to low current-mode operation and internal circuit design

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

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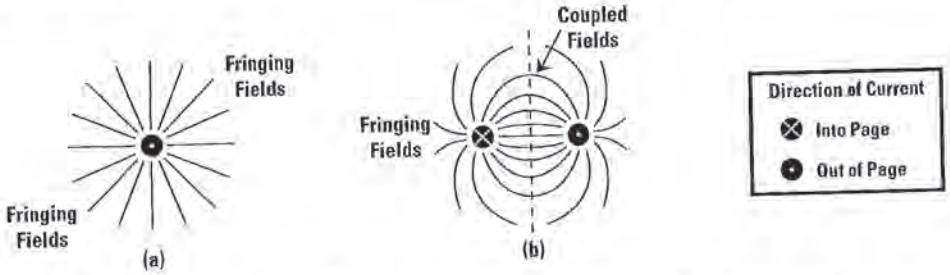
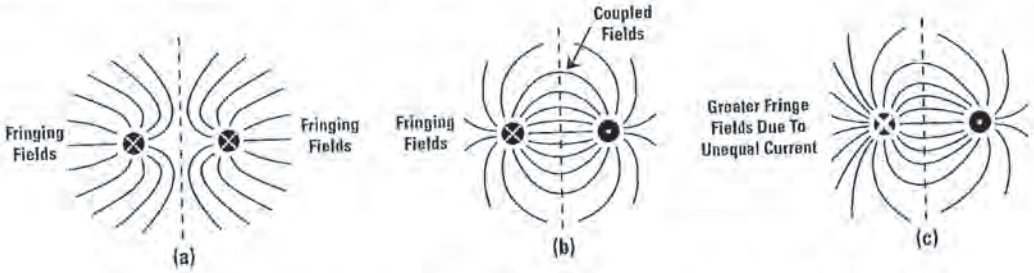
4.3.2 Electromagnetic Radiation of Differential Signals

Today's increasing data rates and tougher electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves which can escape through shielding causing a system to fail EMC tests. Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another). In single-ended lines like CMOS/TTL shown below, almost all the electric field lines are free to radiate away from the conductor. These fields may be intercepted by other objects, but some can travel as TEM waves which may escape the system causing EMI problems.



Electromagnetic field cancellation in differential signals (b) through coupling versus a single-ended signal (a).

Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic fields lines tend to cancel and the electric fields (shown above) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals much less field energy is available to propagate as TEM waves versus single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.



Even or common-mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines.

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in (a) above, but factors can cause an imbalance in currents (c) versus the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

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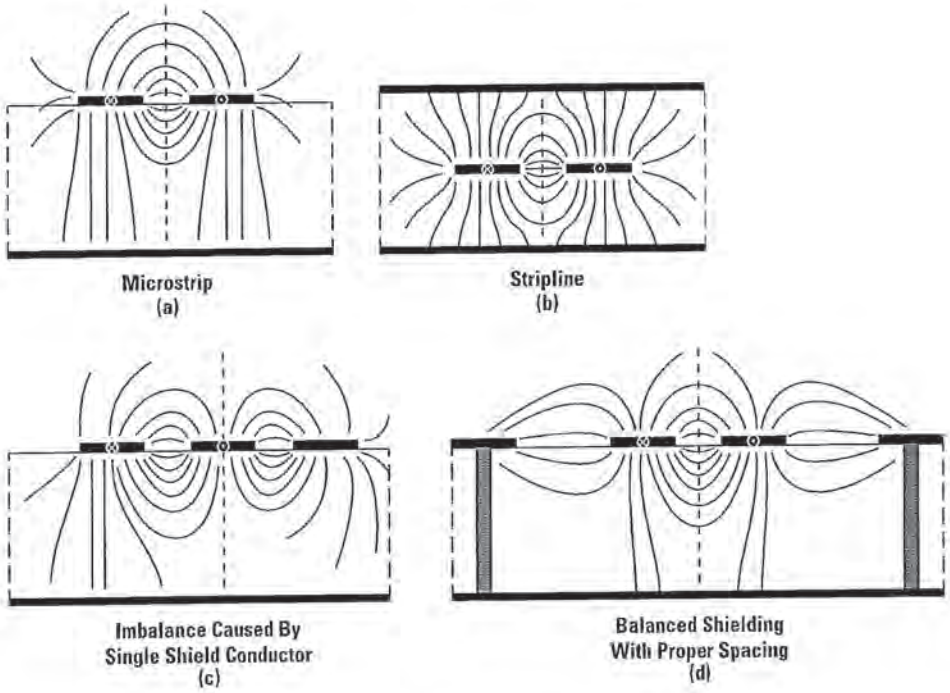
Similar effects can be seen in microstrip and stripline PCB traces shown below. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field.lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_O (Z_{DIFF}). More shielding can be achieved using microstrip without significantly impacting propagation velocity using shield traces as in (d), but be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace — or any trace — on one side (c) creates an imbalance which can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<1/4 wavelength) intervals, and should be placed at least 2S from the pair.



Ideal differential signals on microstrip a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d).

4.3.3 Design Practices for Low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are close coupling between the conductors of each pair and minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown next. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors to preserve closer coupling between the conductors versus the power and ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

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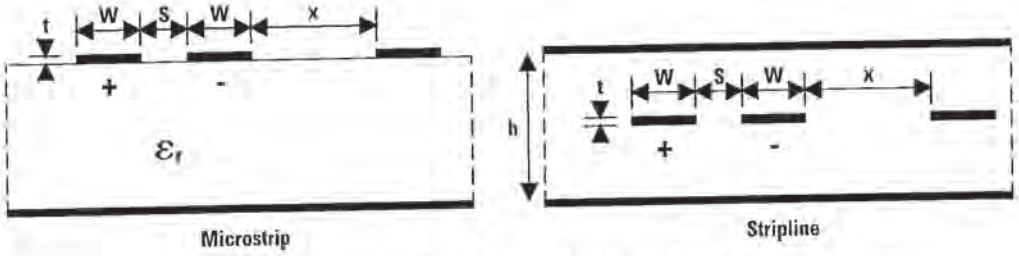
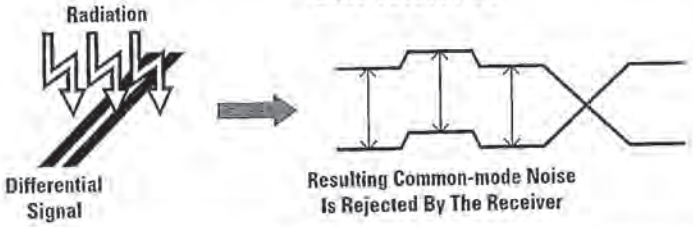


For good coupling, make S < 2W, S < h, and x ≥ 2W & 2S.

For sufficient coupling (canceling) of electromagnetic fields, the distance between the "+" and "–" signal should be minimized.

Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common-mode noise which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.

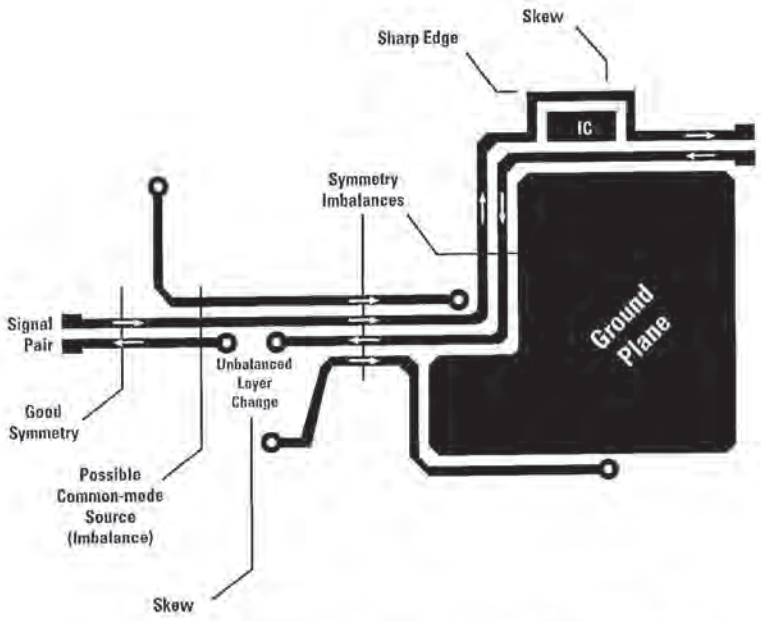
EMI Tolerance



Close coupling not only reduces EMI, but improves EMI tolerance too.

Imbalance minimization is the other important factor in reducing EMI. Although fields result from the complex interaction between objects of a system and are difficult to predict (especially in the dynamic case), certain generalizations can be made. The impedance of your signal traces should be well-controlled. If the impedance of one trace changes versus another, the voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should introduced equally to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, PCB traces, etc. Remember that the key word is balance.



This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation.

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Since fields are proportional to voltage/current amplitude at any given point in time, any factors affecting the time (delay, velocity, etc.) and/or amplitude (attenuation, etc.) properties of the signals can increase EMI and can be seen on a scope. The next figure illustrates how waveforms — easily seen on a scope — can help predict far field EMI. First, the beneficial field canceling effects of ideal differential signals (b) versus single-ended signals (a) are compared.

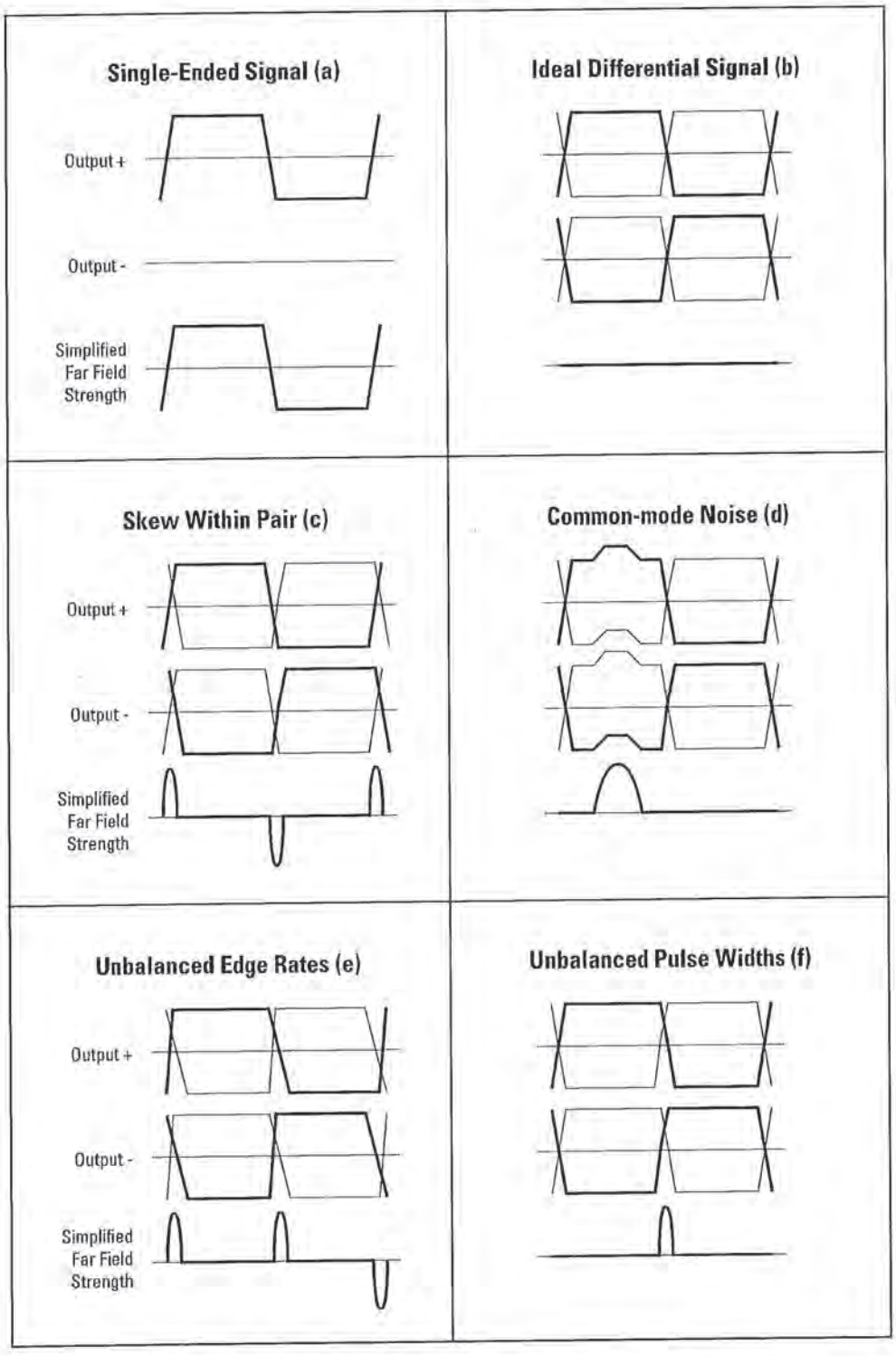
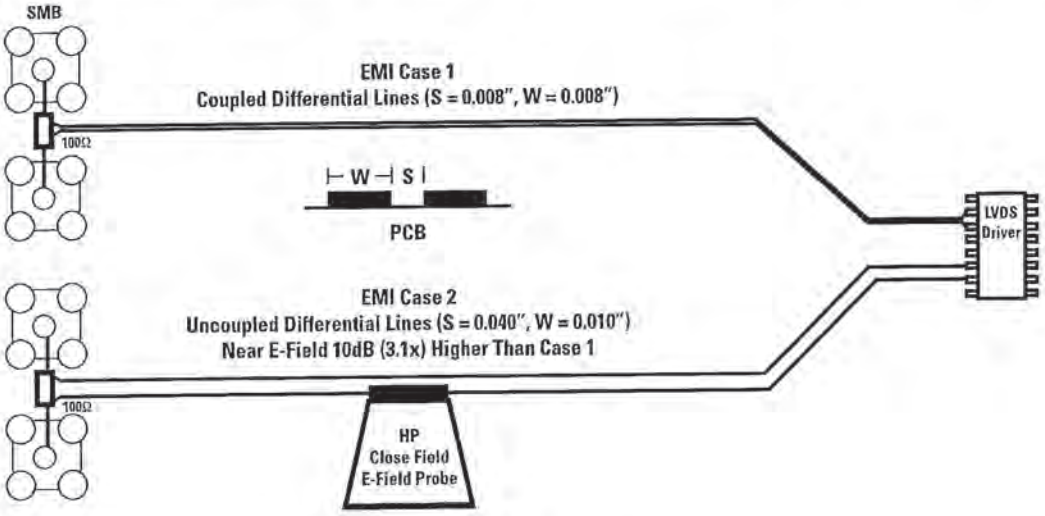


Diagram showing simplified far field radiation under various situations.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common-mode noise, unbalanced attenuation, etc. These affect the relative amplitudes of the fields at any given moment, reducing the canceling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

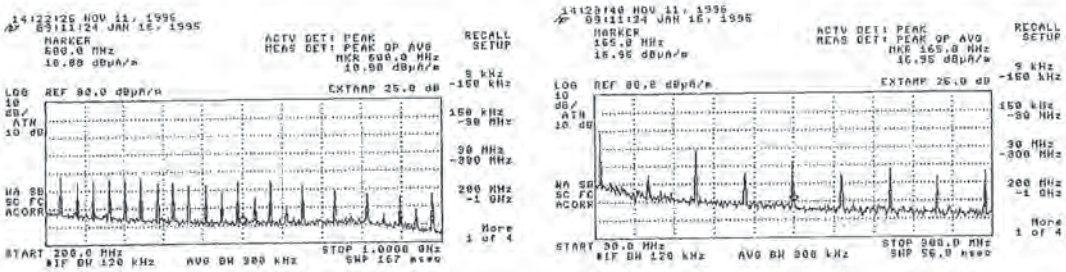
4.3.4 EMI Test Results

The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals versus uncoupled signals. The setup compares two sets of LVDS signals: one set in which pair spacing is less than trace width (S < W) and another set in which S >> W so that the pair members are no longer closely coupled (though the differential impedance of the transmission line is still 100Ω).



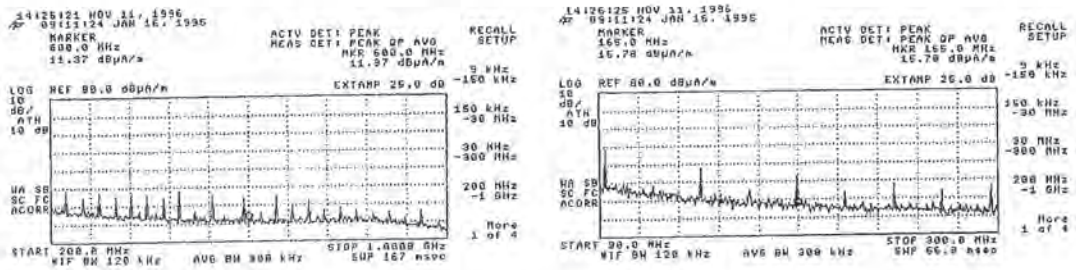
EMI Test Setup

Near (close) field electric field measurements were made for both cases while using a 32.5MHz 50% duty cycle clock as the source. The two plots below show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200MHz to 1GHz. The second plot looks more closely at the frequencies between 30MHz and 300MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.



Near E-Field Strength for Uncoupled Signals
(Case 2): 200MHz-1GHz *(Case 2): 30MHz-300MHz*

The next two plots show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.



Near E-Field Strength for Closely Coupled Signals

(Case 1): 200MHz-1GHz *(Case 1): 30MHz-300MHz*

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The closely coupled pair showed about 10dB (>3 times) lower electric field strength than the uncoupled pair.

This test illustrates two things:

1. Use of differential signals versus single-ended signals can be used effectively to reduce emissions.
2. The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than is seen here.

4.3.5 Ground Return Paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least resistance.

Since LVDS is differential, the signal current that flows in one conductor of a pair will flow back through the other conductor, completing the current loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common-mode noise current which must return also. This common-mode current will be capacitively coupled to ground and return to the driver through the path of least impedance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems.

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common-mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least impedance and means that the current loop area is minimized.

Similarly, in cables, a ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area. (See Chapter 5 on Cables).

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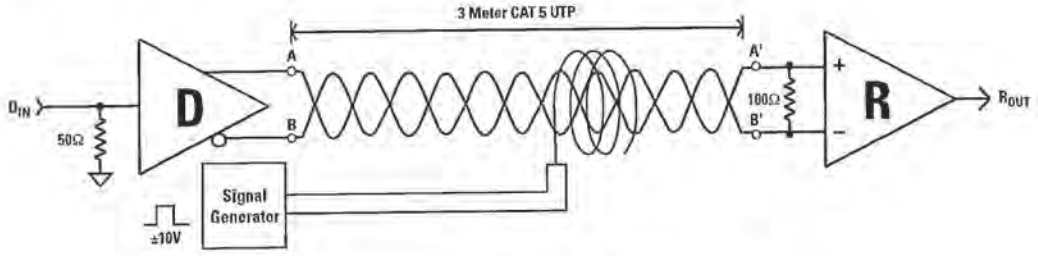
4.3.6 Cable Shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (see Chapter 5).

4.3.7 EMC Conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled and matched.

4.4.0 COMMON-MODE NOISE REJECTION



Common-mode noise rejection test setup.

Test Setup:

Driver: DS90C031 (one channel)
Receiver: DS90C032 (one channel)
V_{CC} = 5V
T_a = 25°C

This test demonstrates the common-mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (±350mV swing with <±100mV thresholds). Provided that the differential signals run close together through controlled impedance media, however, most of the noise on LVDS lines will be common-mode. In other words, EMI, crosstalk, power/ground shifts, etc. will appear equally on each pair and this common-mode noise will be rejected by the receiver. The plots below show common-mode noise rejection with V_{CM} noise up to −0.5V to +3.25V peak-to-peak.

Reference waveform showing LVDS signal and receiver output.

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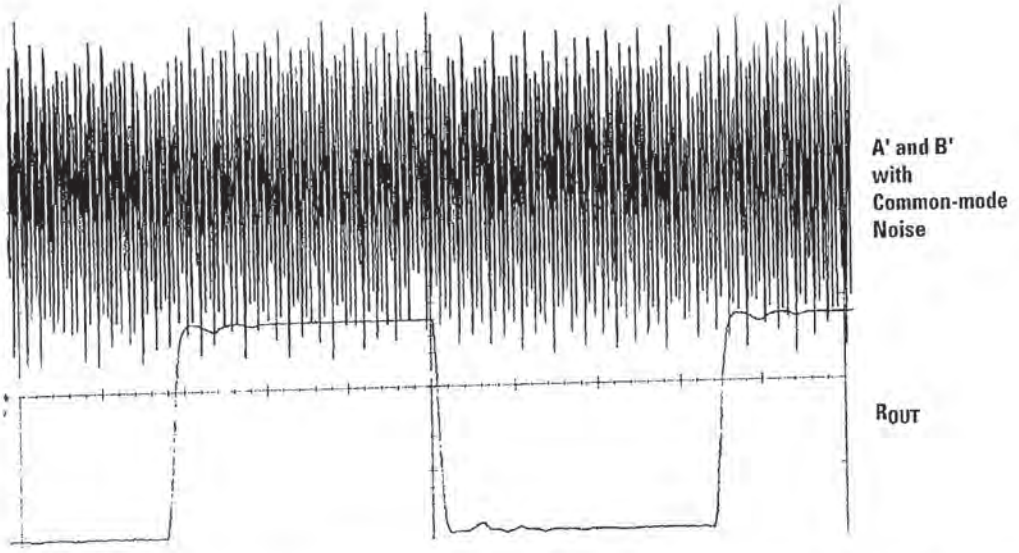
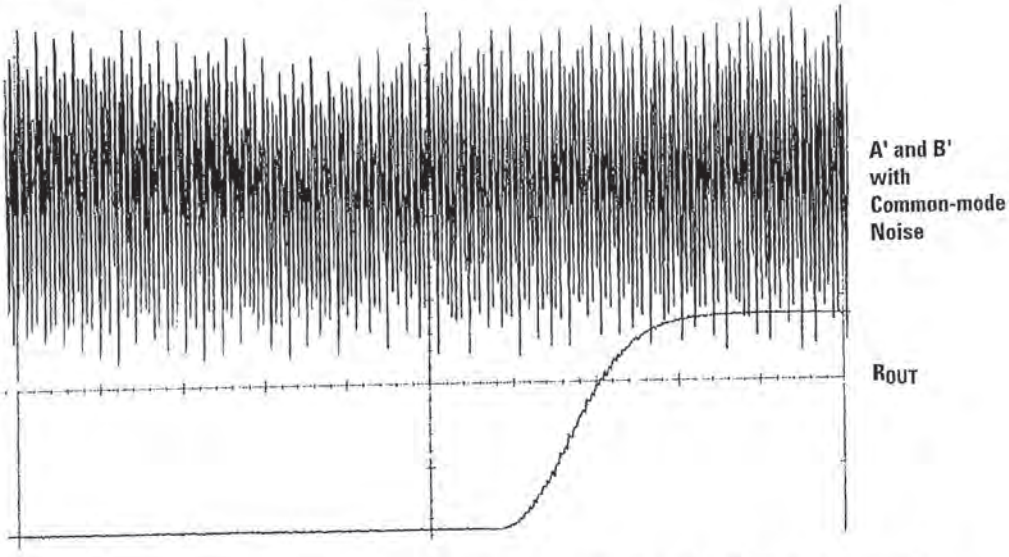


Coupled common-mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output.



Expanded view of coupled common-mode noise waveform and clean receiver output.

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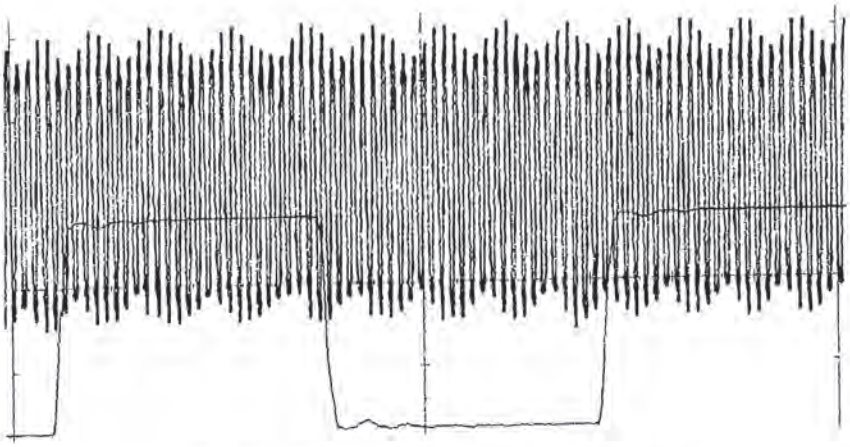


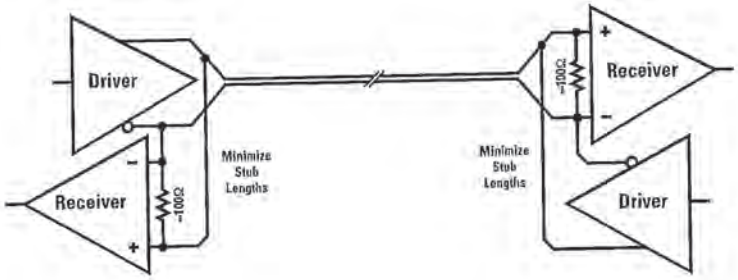
Clean receiver output despite –0.5V to +3.25V peak-to-peak common-mode noise.

4.5.0 LVDS CONFIGURATIONS

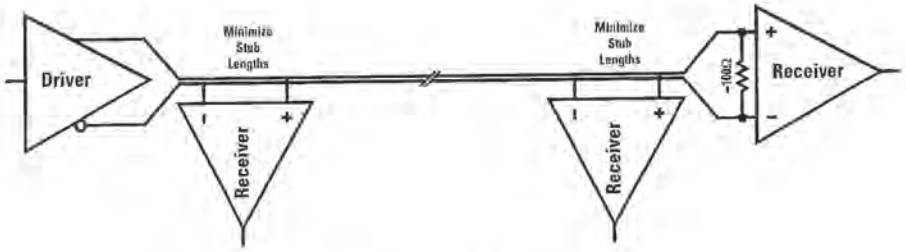
Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The point-to-point configuration does provide the best signal path and should be used for very high-speed interconnect links. Point-to-point links are commonly used in conjunction with crosspoint switches.

The configuration shown below allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin) if using standard LVDS drivers. A better solution would be to employ Bus LVDS (BLVDS) drivers which are designed for double termination loads. They provide levels compatible with LVDS and do not trade off noise margin. Common-mode range for LVDS and BLVDS is ±1V (typical), so cable lengths tend to be in the tens of meters.

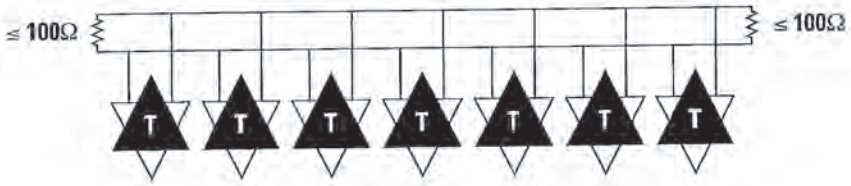


Bi-directional half-duplex configuration.



Multidrop configuration.

Since LVDS receivers have high impedance inputs, a multidrop configuration can also be used if transmission distance is short and stub lengths are less than ~12mm (as short as possible). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down. This application is good when the same set of data needs to be distributed to multiple locations.



Multipoint Configuration.

A multipoint bus supports multiple drivers, but only one is allowed to be active at any given time. With Bus LVDS devices, double terminated busses can be used without trading off signal swing and noise margin. Termination should be located at both ends of the bus. Failsafe biasing should be considered if a known state on the bus is required when all drivers are in TRI-STATE®. As with the multidrop bus, stubs off the mainline should be kept as short as possible to minimize transmission line problems.

4.6.0 FAILSAFE BIASING OF LVDS

4.6.1 Most Applications

Most LVDS receivers have internal failsafe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Always consult the component's datasheet to determine which type of failsafe protection is supported. Here is a summary of LVDS failsafe conditions:

OPEN INPUT PINS - Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state. This minimizes power dissipation and switching noise.

TERMINATED INPUT PINS - If the cable is removed and the inputs to the receiver have a termination resistor across them, then the output will be stable (HIGH). Noise picked up at the input, if differential in nature, can cause the device to respond. If this is the case see section 4.6.2 below.

TERMINATED INPUT PINS - Noisy Environments - See section 4.6.2 if failsafe must be guaranteed in noisy environments when the cable is disconnected from the driver's end or if the driver is in TRI-STATE®.

SHORTED INPUTS - The receiver output will remain in a high state when the inputs are shorted. This is considered a fault condition protection only. It is not specified across the input voltage range of the receiver.

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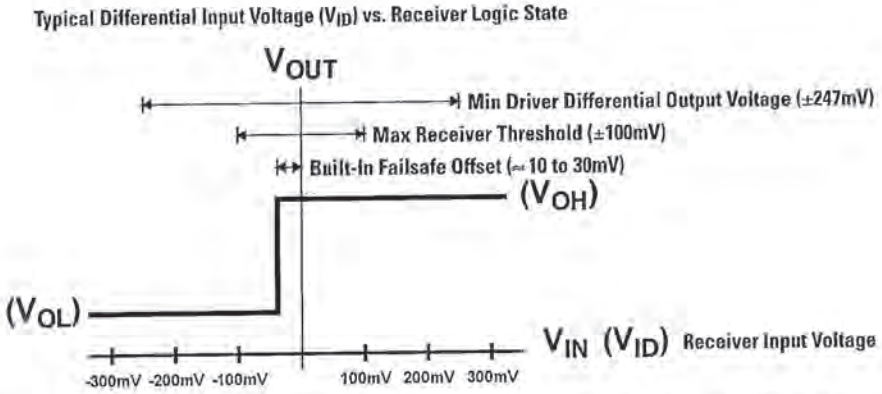
4.6.2 Boosting Failsafe In Noisy Environments

The internal failsafe circuitry is designed to source/sink a very small amount of current, providing failsafe protection for floating receiver inputs, shorted receiver inputs, and terminated receiver inputs as described above and in the component's datasheet. It is not designed to provide failsafe in noisy environments when the cable is disconnected from the driver's end or if the driver is in TRI-STATE®. When this happens, the cable becomes a floating antenna which can pick up noise. If the cable picks up more differential noise than the internal failsafe circuitry can overcome, the receiver may switch or oscillate. If this condition can happen in your application, it is recommended that you choose a balanced and/or shielded cable which will reduce the amount of differential noise on the cable. In addition, you may wish to add external failsafe resistors to create a larger noise margin. However, adding more failsafe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore, a compromise should be the ultimate goal.

4.6.3 Choosing External Failsafe Resistors



External failsafe can be added, but must be small enough not to significantly affect driver current.

The chart above shows that National's present LVDS devices typically have an internal failsafe voltage of about -10 to -30mV. If the receiver will not always be driven by the driver in your application and the cable is expected to pick up more than 10mV of differential noise you may need to add additional failsafe resistors. The resistors are chosen by first measuring/predicting the amount of differential-mode noise you will need to overcome. V_{FSB} is the offset voltage generated across the termination resistor (100Ω). Note that you do not need to provide a bias (V_{FSB}) which is greater than the receiver threshold (100mV), typically +15mV or +20mV is sufficient. You only need enough to overcome the differential noise, since the internal failsafe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

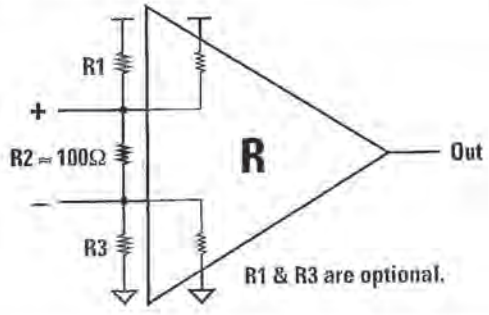


Diagram showing simplified internal failsafe circuitry and optional external "helper" failsafe resistors.

For best results, follow these procedures when choosing external failsafe resistors:

1. First ask the question "Do I need external failsafe?" If your LVDS driver is always active, you will not need external failsafe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential-mode noise, you may not need to boost failsafe.

2. Measure/predict the amount of differential-mode noise at the receiver end of the cable in worst case conditions. If you have a lot of noise, use a balanced cable like twisted pair which tends to pick up mostly common-mode noise, not differential-mode noise. Do not use simple ribbon cables which can pick up differential-mode noise due to fixed positions of the conductors.

   Use a shielded cable if possible. Using a balanced and/or shielded cable is best way to prevent noise problems in noisy environments.

3. Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst case conditions. Set this equal to V_{FSB} in the equation below and solve for the external failsafe resistors R1 and R3.

$$V_{FSB} = \frac{R2}{R1 + R2 + R3} V_{CC}$$

$$I_{BIAS} = \frac{V_{CC}}{R1 + R2 + R3} << I_{LOOP} \quad (\text{Use } I_{BIAS} \leq 0.1 * I_{LOOP})$$

$$V_{CM} = \frac{R3 + R2/2}{R1 + R2 + R3} V_{CC} = 1.2V \Rightarrow R1 \approx R3 \left(\frac{V_{CC}}{1.2V} - 1 \right)$$

$$R_{TEQ} = \frac{R2\,(R1 + R3)}{R1 + R2 + R3} = \text{match transmission line } Z_{ODIFF}$$

4. You now have an equation relating R1 to R3. Choose R1 and R2 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current (I_{BIAS} << I_{LOOP}, equation two). In general, R1 and R2 should be greater than 20kΩ for V_{CC} = 5V and greater than 12kΩ for V_{CC} = 3.3V. Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.

5. The external failsafe resistors may change your equivalent termination resistance, R_{TEQ}. Fine tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

4.7.0 POWER-OFF HIGH IMPEDANCE BUS PINS

Power off high impedance is a useful feature, most 2nd and 3rd generation LVDS receivers provide this feature. This is typically listed as a feature and also as a condition of the I_{IN} parameter. This feature is useful in applications that employ more than one receiver and they are powered from local power supplies. If the power is turned off to one node, it should not load down the line and prevent communication between other powered-up nodes.

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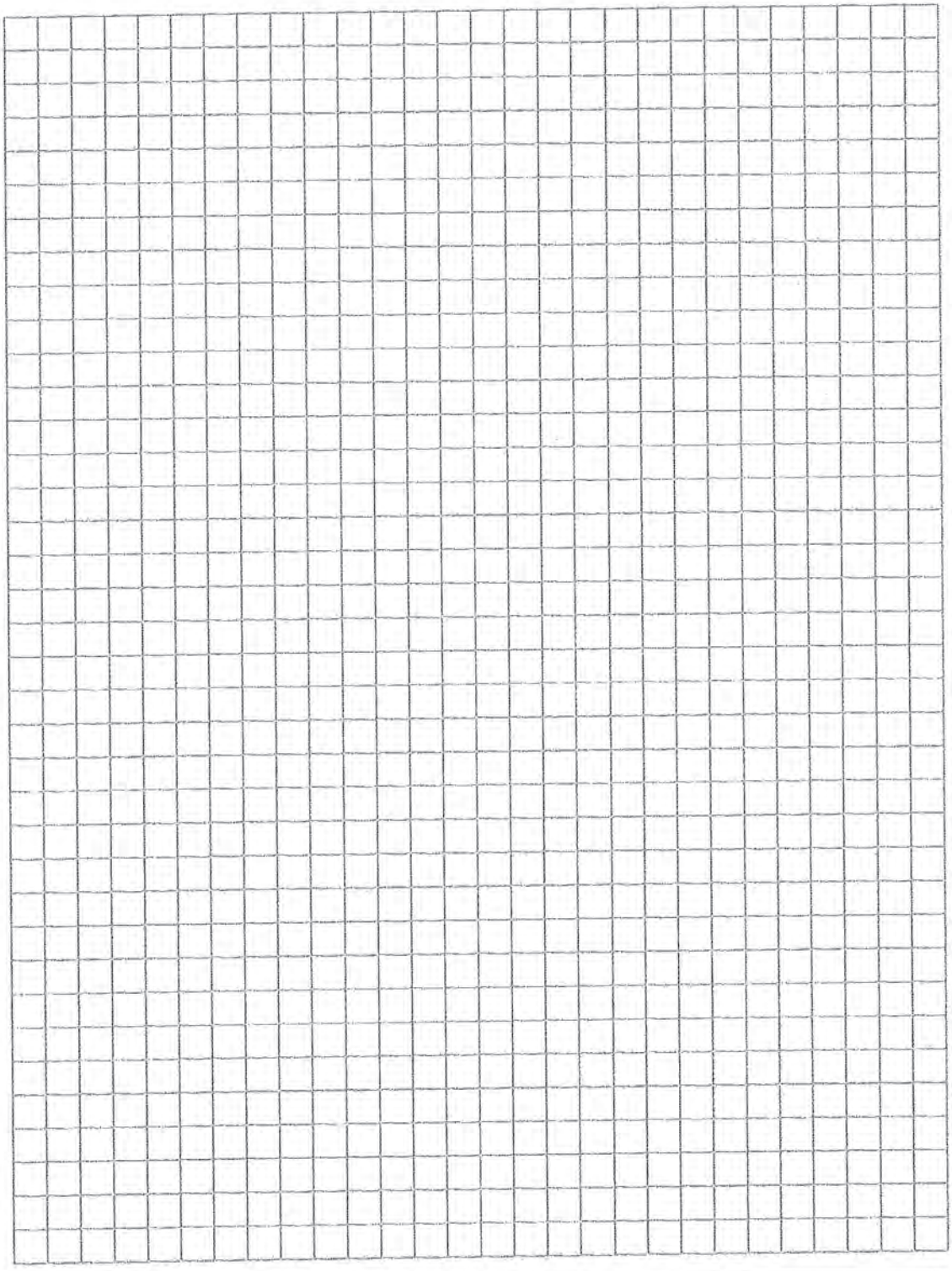
NOTES



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Cables, Connectors and Performance Testing

Chapter 5

5.0.0 CABLES, CONNECTORS AND PERFORMANCE TESTING

5.1.0 GENERAL COMMENTS

When choosing cables and connectors for LVDS it is important to remember:

1. Use controlled impedance media. The cables and connectors you use should have a differential impedance of about 100Ω. They should not introduce major impedance discontinuities that cause signal reflections.

2. Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential-mode) noise, which is rejected by the receiver.

3. For cable distances < 0.5m, most cables can be made to work effectively. For distances 0.5m < d < 10m, CAT 3 (Category 3) twisted pair cable works well and is readily available and relatively inexpensive. Other types of cables may also be used as required by a specific application. This includes twin-ax cables built from separate pairs and ribbon style constructions, which are then coiled.

5.2.0 CABLING SUGGESTIONS

As described above, try to use balanced cables (twisted pair, twin-ax, or flex circuit with closely coupled differential traces). LVDS was intended to be used on a wide variety of media. The exact media is not specified in the LVDS Standard, as it is intended to be specified in the referencing standard that specifies the complete interface. This includes the media, data rate, length, connector, function, and pin assignments. In some applications that are very short (< 0.3m), ribbon cable or flex circuit may be acceptable. In box-to-box applications, a twisted pair or twin-ax cable would be a better option due to robustness, shielding and balance. Whatever cable you do choose, following the suggestions below will help you achieve optimal results.

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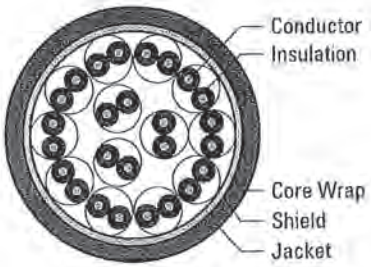
5.2.1 Twisted Pair



Drawing of Twisted Pair Cable, Cross-Section

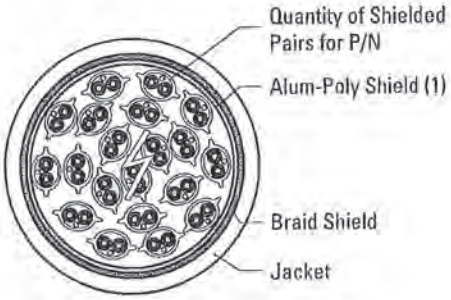
Twisted pair cables provide a good, low cost solution with good balance, are flexible, and capable of medium to long runs depending upon the application skew budget. It is offered with an overall shield or with shields around each pair as well as an overall shield. Installing connectors is more difficult due to its construction.

a) Twisted pair is a good choice for LVDS. Category 3 (CAT3) cable is good for runs up to about 10m, while CAT5 has been used for longer runs.

b) For the lowest skew, group skew-dependent pairs together (in the same ring to minimize skew between pairs).

c) Ground and/or terminate unused conductors (do not float).

5.2.2 Twin-ax Cables



Drawing of Individually Shielded Parallel Pair Twin-ax Cable - Cross Section

Twin-ax cables are flexible, have low skew and shields around each pair for isolation. Since they are not twisted, they tend to have very low skew within a pair and between pairs. These cables are for long runs and have been commonly deployed in Channel Link and FPD-Link applications.

a) Drain wires per pair may be connected together in the connector header to reduce pin count.

b) Ground and/or terminate unused conductors.

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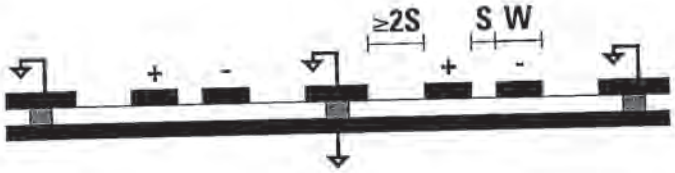
5.2.3 Flex Circuit

Flex circuit is a good choice for very short runs, but it is difficult to shield. It can be used as an interconnect between boards within a system.



Flex Circuit - Cross-Section

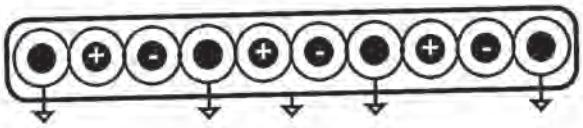
a) Closely couple the members of differential pairs (S < W). Do not run signal pairs near the edges of the cable, as these are not balanced.

b) Use a ground plane to establish the impedance.

c) Use ground shield traces between the pairs if there is room. Connect these ground traces to the ground plane through vias at frequent intervals.

5.2.4 Ribbon Cable

Ribbon cable is cheap and is easy to use and shield. Ribbon cable is not well suited for high-speed differential signaling (good coupling is difficult to achieve), but it is OK for very short runs.



Flat Cable - Cross-Section

a) If ribbon cable must be used, separate the pairs with ground wires. Do not run signal pairs at the edges of the ribbon cable.

b) Use shielded cable if possible, shielded flat cable is available.

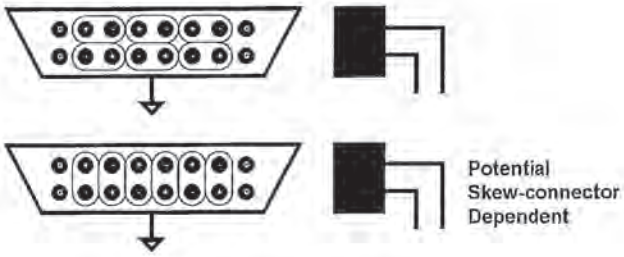
5.2.5 Additional Cable Information

Additional information on cable construction may be found in National Application Note AN-916. Also, many cable, connector and interconnect system companies provide detailed information on their respective websites about different cable options. A non-inclusive list of a few different options is provided below:

3M	www.3M.com/interconnects/
Spectra-Strip Cable Products	www.spectra-strip.amphenol.com/default.CFM
AMP	http://connect.amp.com/

5.2.6 Connectors

Connectors are also application dependent and depend upon the cable system being used, the number of pins, the need for shielding and other mechanical footprint concerns. Standard connectors have been used at low to medium data rates, and optimized low skew connectors have been developed for medium to high-speed applications.



Typical Connector Pinouts

a) Choose low skew, impedance matching connectors if possible.

b) Group members of each pair together. Pins of a pair should be close together (adjacent) not separated from each other. This is done to maintain balance, and to help ensure that external noise, if picked up, will be common-mode and not differential in nature.

c) Some connectors have different length leads for different pins. Group pairs on same length leads. Consult the connector manufacturer for the orientation of pins that yield the lowest skew and crosstalk for your particular connector. Shorter pin lengths tend to be better than long ones, minimize this distance if possible.

d) Place ground pins between pairs where possible and convenient. Especially use ground pins to separate TTL/CMOS signals for LVDS signals.

e) Ground end pins. Do not use end pins for high-speed signals, if possible, as they offer less balance.

f) Ground and/or terminate unused pins.

Many different connector options exist. One such cable-connector system that has been used for LVDS with great results is the 3M "High-speed MDR Digital Data Transmission System." This cable system is featured on the National Channel-Link (48-bit) and LDI Evaluation Kits. The connector is offered in a surface mount option that has very small skew between all the pins. Different cable types are also supported.

5.3.0 CABLE GROUND AND SHIELD CONNECTIONS

In many systems, cable shielding is required for EMC compliance. Although LVDS provides benefits of low EMI when used properly, shielding is still usually a good idea especially for box-to-box applications. Together, cable shielding and ground return wires help reduce EMI. The shielding contains the EMI and the ground return wire (the pair shield or drain wire in some cables) and provides a small loop area return path for common-mode currents. Typically one or more pairs are assigned to ground (circuit common). Using one or more pair reduces the DCR (DC Resistance) of the path by the parallel connection of the conductors. This provides a known, very low impedance return path for common-mode currents.

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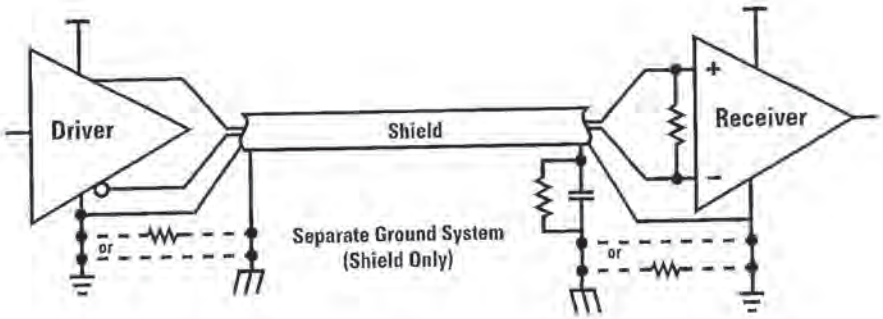

Typical Grounding Scheme

In most applications the grounding system will be common to both the receiver and the driver. The cable shield is connected at one end with a DC connection to the common ground (frame ground). Avoid "pig-tail" (high inductance) ground wiring from the cable. The other end of the shield is typically connected with a capacitor or network of a capacitor and a resistor as shown in the above example. This prevents DC current flow in the shield. In the case where connectors are involved that penetrate the system's enclosure, the cable shield must have a circumferential contact to the connector's conductive backshell to provide an effective shield and must make good contact.

Note: It is beyond the scope of this book to effectively deal with cabling and grounding systems in detail. Please consult other texts on this subject and be sure to follow applicable safety and legal requirements for cabling, shielding and grounding.

5.4.0 LVDS SIGNAL QUALITY

Signal quality may be measured by a variety of means. Common methods are:

- Measuring rise time at the load
- Measuring Jitter in an Eye Pattern
- Bit Error Rate Testing
- Other means

Eye Patterns and Bit Error Rate Testing (BERT) are commonly used to determine signal quality. These two methods are described next.

5.4.1 LVDS Signal Quality: Jitter Measurements Using Eye Patterns

This report provides an example of a data rate versus cable length curve for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and the printed circuit boards (PCB). Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment — or even better — in the actual application. Eye pattern measurements are useful in measuring the amount of jitter versus the unit internal to establish the data rate versus cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

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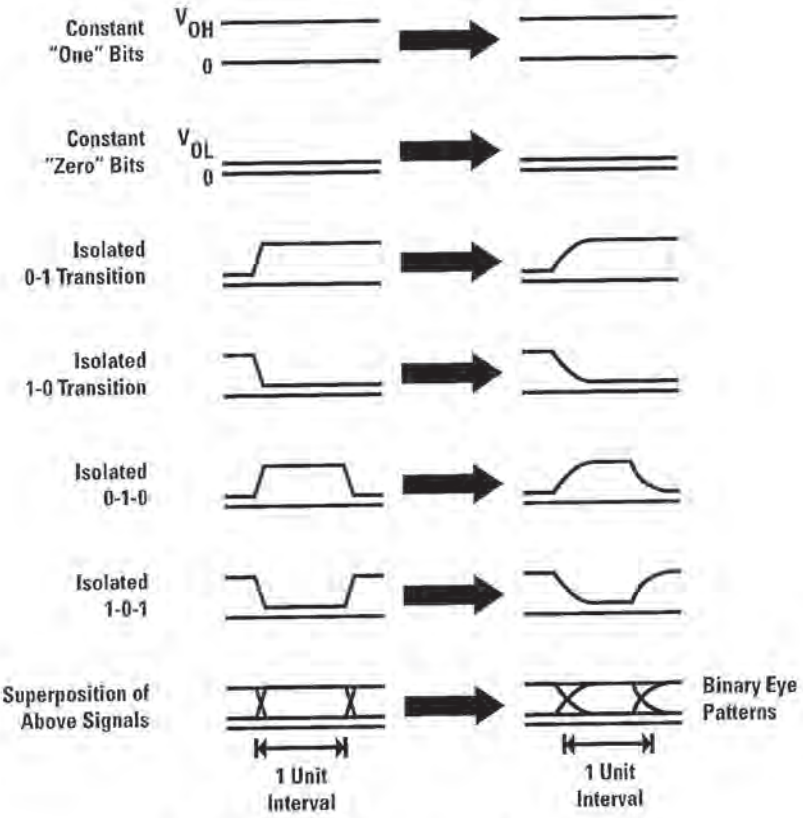
5.4.2 Why Eye Patterns?

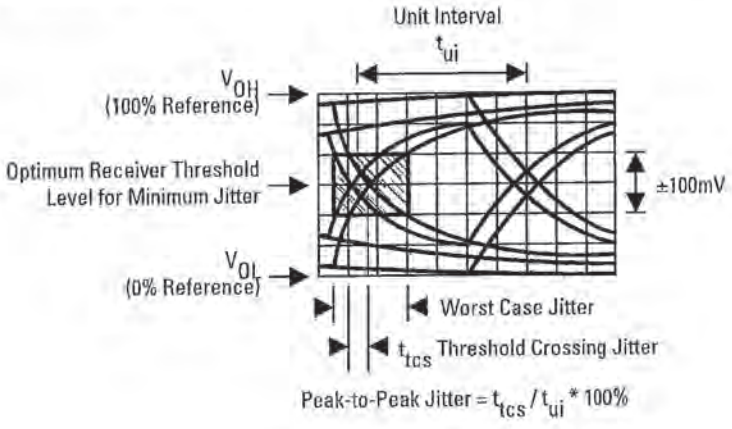
The eye pattern is used to measure the effects of inter-symbol interference on random data being transmitted through a particular medium. The prior data bits effect the transition time of the signal. This is especially true for NRZ data that does not guarantee transitions on the line. For example in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects of the cable. The next figure illustrates the superposition of six different data patterns. Overlaid, they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider and the opening of the eye is also now smaller (see application note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter-symbol distortion as is a data line.



Formation of an Eye Pattern by Superposition.

The figure below describes the measurement locations for minimum jitter. Peak-to-Peak Jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between −100mV and +100mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100mV and the jitter measured between the first and last crossing at ±100mV. If the vertical axis units in the figure were 100mV/division, the worse case jitter is at ±100mV levels.



NRZ Data Eye Pattern.

5.4.3 Eye Pattern Test Circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in the figure below. This figure details the test circuit that was used to acquire the Eye pattern measurements. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: The cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential-mode) 28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report, the following cable lengths were tested: 1, 2, 3, 5, and 10 meter(s). Cables longer that 10 meters were not tested, but may be employed at lower data rates.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

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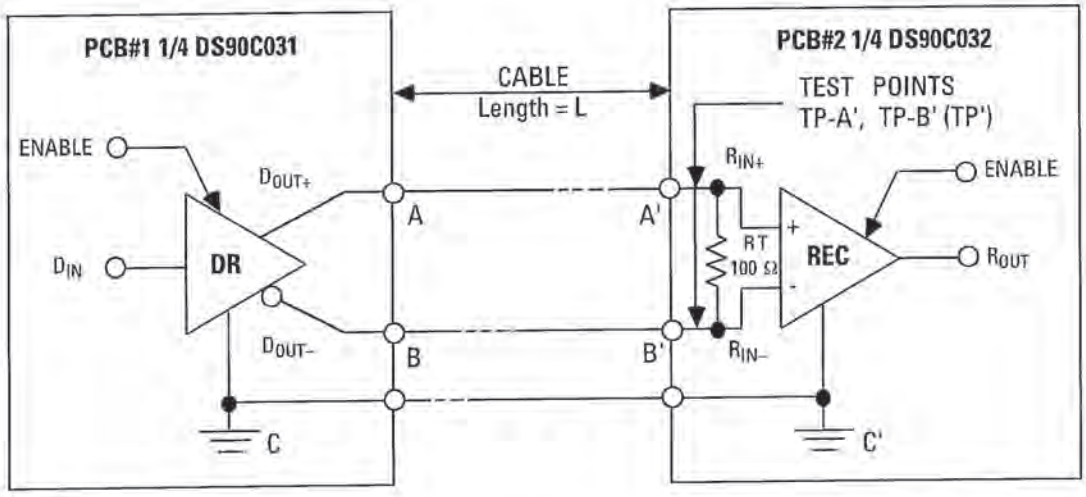

LVDS Signal Quality Test Circuit

5.4.4 Test Procedure

A pseudo-random (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. Jitter was first measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone and although this will result in a much lower jitter point, it ignores the fact that the receivers may not switch at that very point. For this reason, this signal quality test report measured jitter at both points.

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5.4.5 Results and Data Points

20% Jitter Table @ 0V Differential (Minimum Jitter)

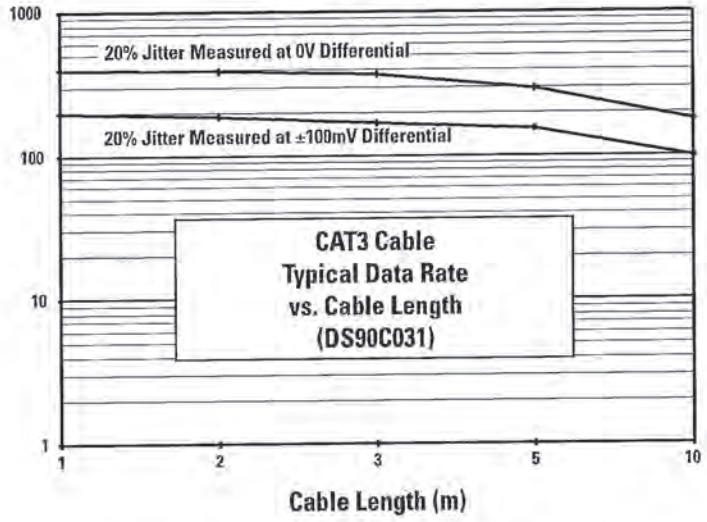
Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, Jitter was measured at the 0V differential point. For the case with the 1 meter cable, 490ps of jitter at 400Mbps was measured, and with the 10 meter cable, 1.160ns of jitter at 180Mbps was measured.

20% Jitter Table @ ±100 mV (Maximum Jitter)

Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100mV levels. For the 1 meter cable, 1ns of jitter was measured at 200Mbps, and for the 10 meter cable, 2ns of jitter occurred at 100Mbps.



Typical Data Rate vs Cable Length for 0-10m CAT3 Cable

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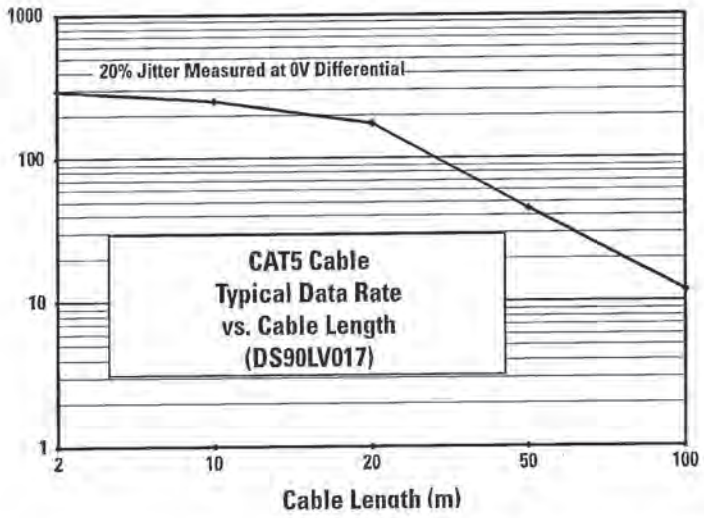

Typical Data Rate vs Cable Length for 2-100m CAT5 Cable (See AN-1088)

Care should be taken in long cable applications using LVDS. When directly coupled, LVDS provides up to ±1V common-mode rejection. Long cable applications may require larger common-mode support. If this is the case, transformer coupling or alternate technologies (such as RS-485) should be considered.

The figures above are a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200-400 Mbps are possible at shorter lengths, and rates of 100-200Mbps are possible at 10 meters. Note that employing a different coding scheme, cable, wire gauge (AWG), etc. will create a different relationship between maximum data rate versus cable length. Designers are greatly encouraged to experiment on their own.

5.4.6 Additional Data on Jitter & Eye Patterns

For additional information on LVDS "Data Rate vs Cable Length" please consult the list of LVDS application notes on the LVDS web site at: **www.national.com/appinfo/lvds/**

At this time of this printing the following application notes were available:

AN#	Devices Tested
AN-977	DS90C031/032
AN-1088	DS90LV017/027, DS92LV010A

5.4.7 Conclusions – Eye Pattern Testing

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate versus distance for a common, inexpensive type of cable.

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5.5.0 BIT ERROR RATE (BER) TESTING

Bit error rate testing is another approach to determine signal quality. This test method is described next.

5.5.1 LVDS Cable Driving Performance using BERT

The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example — see application note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector and information about the printed circuit boards (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and Bit Error Rate tests (BER).

This report provides the results of a series of Bit Error Rate tests performed on the DS90C031/032 LVDS Quad Line driver/receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1 to 5 meters of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

5.5.2 What is a BER Test?

Bit Error Rate testing is one way to measure of the performance of a communications system. The standard equation for a bit error rate measurement is:

Bit Error Rate = (Number of Bit errors)/(Total Number of Bits)

Common measurement points are bit error rates of:

$\leq 1 \times 10^{-12}$ => One or less errors in 1 trillion bits sent

$\leq 1 \times 10^{-14}$ => One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance benchmark. For example, if the data rate is 50Mbps, and the benchmark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

5.5.3 BER Test Circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in the next figure. This figure details the test circuit that was used. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential-mode) 28 AWG stranded twisted pair cable (25 Pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report, cable lengths of 1 and 5 meters were tested.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

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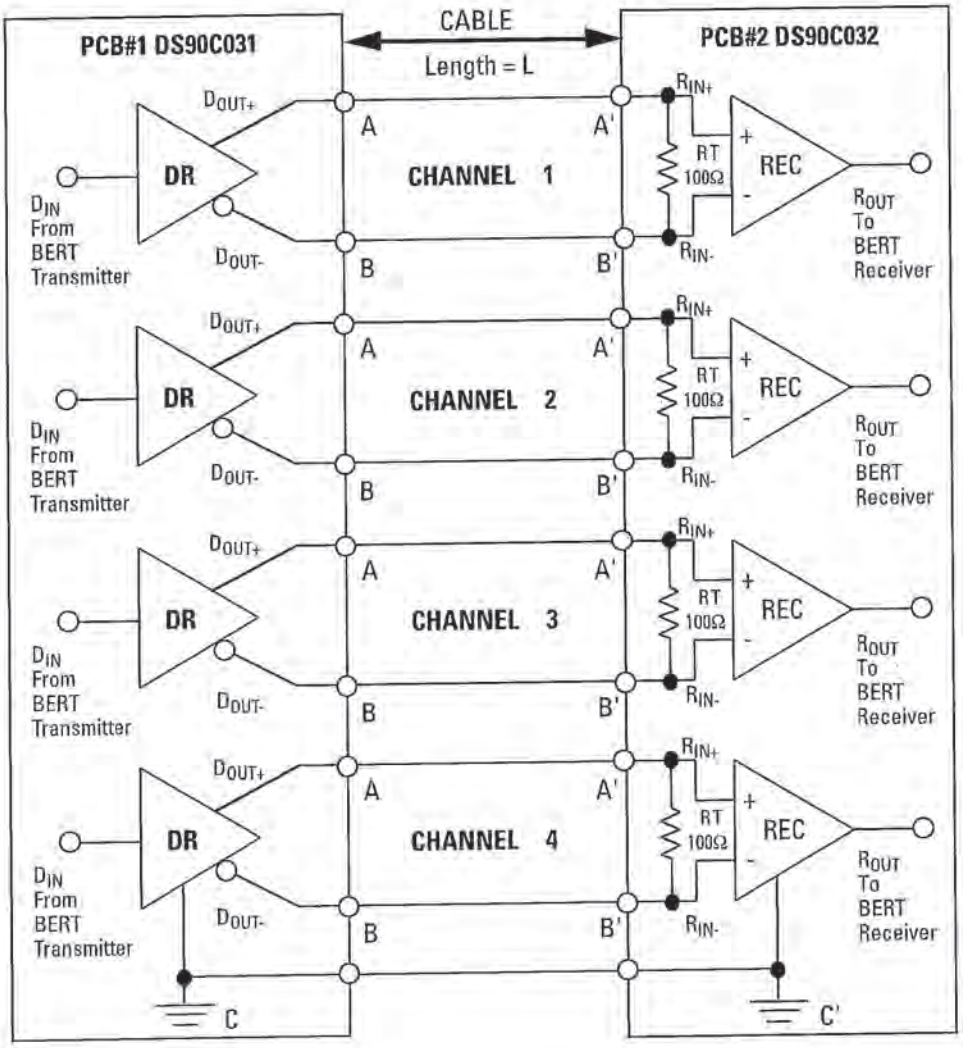

LVDS BER Test Circuit

5.5.4 Test Procedure

A parallel high-speed BER transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The BER tester was configured to provide a PRBS (Pseudo Random Bit Sequence) of 2^{15}-1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4-bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block, the results were recorded which included: elapsed seconds, total bits transmitted and number of bit errors recorded. For the three tests documented next, a power supply voltage of +5.0V was used and the tests were conducted at room temperature.

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5.5.5 Tests and Results

The goal of the tests was to demonstrate errors rates of less than 1×10^{-12} are obtainable.

TEST #1 Conditions:

Data Rate = 50Mbps
Cable Length = 1 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

TEST #1 Results:

Total Seconds: 87,085 (1 day)
Total Bits: $1{,}723 \times 10^{13}$
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

TEST #2 Conditions:

Data Rate = 100Mbps
Cable Length = 1 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #2 Results:

Total Seconds: 10,717 (~3 hr.)
Total Bits: 4.38×10^{12}
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

TEST #3 Conditions:

Data Rate = 100Mbps
Cable Length = 5 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #3 Results:

Total Seconds: 10,050 (~2.8 hr.)
Total Bits: 4×10^{12}
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

5.5.6 Conclusions - BERT

All three of the tests ran error free and demonstrate extremely low bit error rates using LVDS technology. The tests concluded that error rates of $< 1 \times 10^{-12}$ can be obtained at 100Mbps operation across 5 meters of twisted pair cable. BER tests only provide a "Go — No Go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in the tests conducted by increasing the cable length from 1 meter to 5 meters, and also adjusting the data rate from 50Mbps to 100Mbps. Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and by applying heat/cold to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e. 24 hours). BER tests conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.

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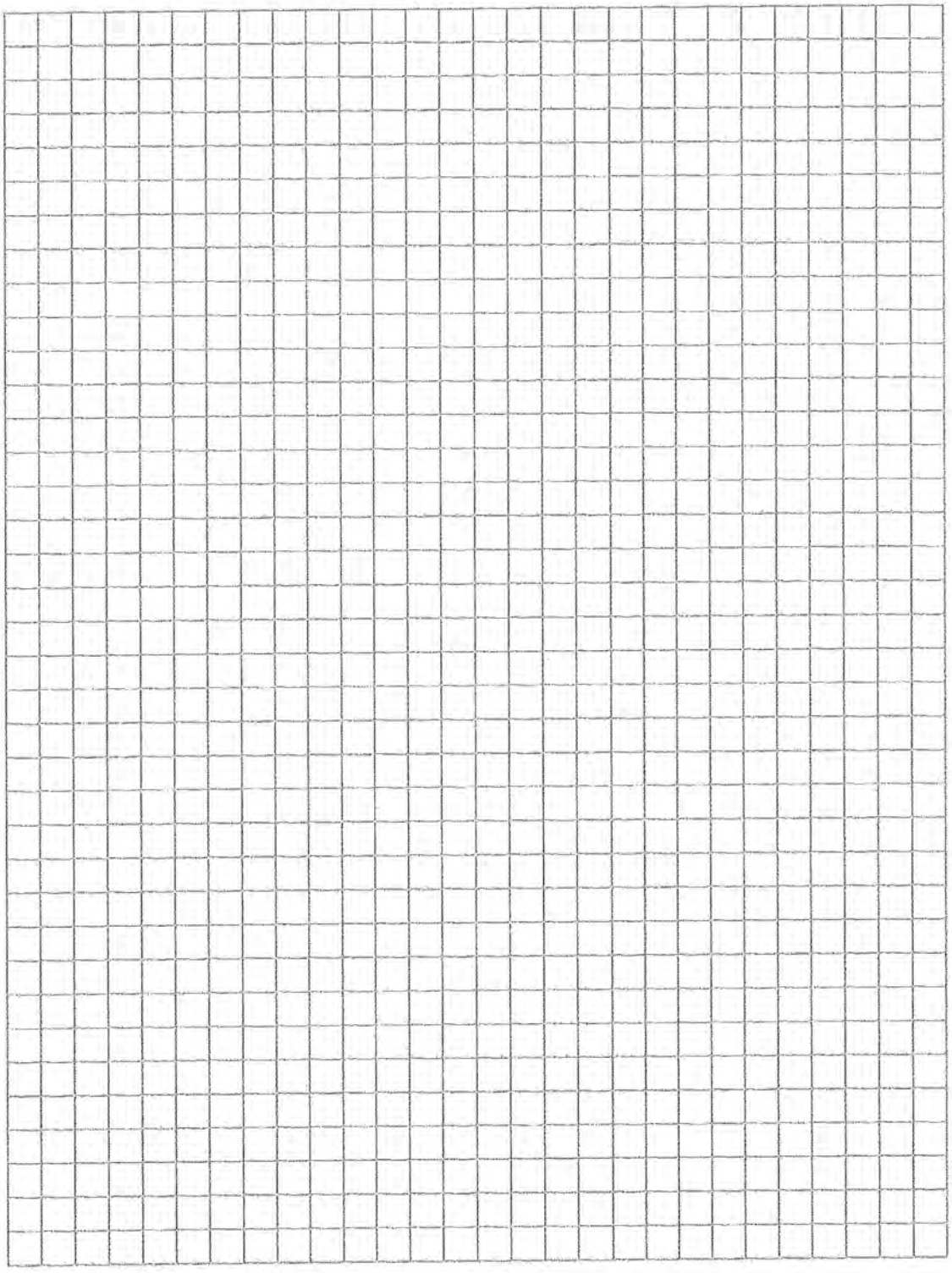
NOTES



Backplane Design Considerations and Bus LVDS

Chapter 6

6.0.0 BACKPLANE DESIGN CONSIDERATIONS AND BUS LVDS

Many high-speed applications require more than just the ability to run point-to-point or from one driver to multiple receivers. Multiple driver(s) and/or receiver(s) on one interconnect is an efficient and common bus application. This requires a double termination of the interconnect to properly terminate the signal at both ends of the bus. Multipoint configurations offer an efficient balance between interconnect density and throughput. LVDS drivers are not intended for double termination loads, thus an enhanced family of devices was invented by National to bring the advantages of LVDS to bus applications.

For multidrop (with the driver located in the middle) and multipoint applications, the bus normally requires termination at both ends of the media. If the bus were terminated with 100Ω at both ends, a driver in the middle would see an equivalent load of 50Ω. Depending upon the load spacing, the effective impedance of the bus may drop further, and for signal quality reasons, the terminations may be as low as 60Ω. Again, a driver would see both resistors in parallel, thus a 30Ω load.

Standard (644) LVDS drivers have only 3.5mA of loop current. If these were used to drive the doubly terminated bus with a termination load of 30Ω, they would only generate a 105mV differential voltage on the bus. This small differential voltage is not sufficient when noise margins, reflections, over-drive and signal quality are taken into account. In fact, even doubling the drive is not enough for a heavily loaded backplane application.

Bus LVDS addresses the issue of driving a low impedance interconnect by boosting its driver current to about 10mA. This means that into a load as low as 30Ω, a 300mV differential signal is maintained. Thus, LVDS-like signaling with all of its benefits is obtained in doubly terminated bus applications.

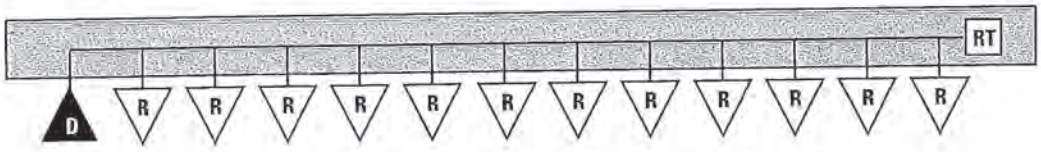
6.1.0 CONFIGURATIONS

Backplanes present special challenges to data transmission systems. This is due to the variety of interconnections (multidrop, multipoint, and switch fabrics) and also the close spacing of the loads. For these very reasons, National invented the Bus LVDS family of interface devices to extend the benefits of LVDS into backplane applications which commonly require two terminations.

There are a number of ways of implementing high-speed backplanes. Each of these ways of implementing a backplane has advantages and disadvantages.

6.1.1 Multidrop (Single Termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that the driver is restricted to be located at one end of the bus and the other end is terminated. This configuration is useful for data distribution applications and may employ standard LVDS or Bus LVDS devices.



Multidrop Application with a Single Termination

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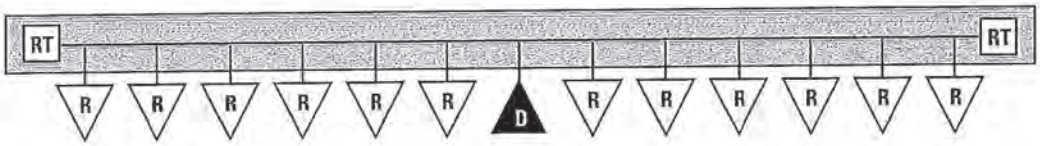
This architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces) which in many cases reduces the stack up of the backplane to fewer layers.

A disadvantage of this configuration is the restricted location of the driver, and (if required) complexity of a back channel (communication path from the loads back to the source).

6.1.2 Multidrop (Double Termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that with Bus LVDS, the driver can be placed anywhere in the multidrop bus and the bus is terminated at both ends.

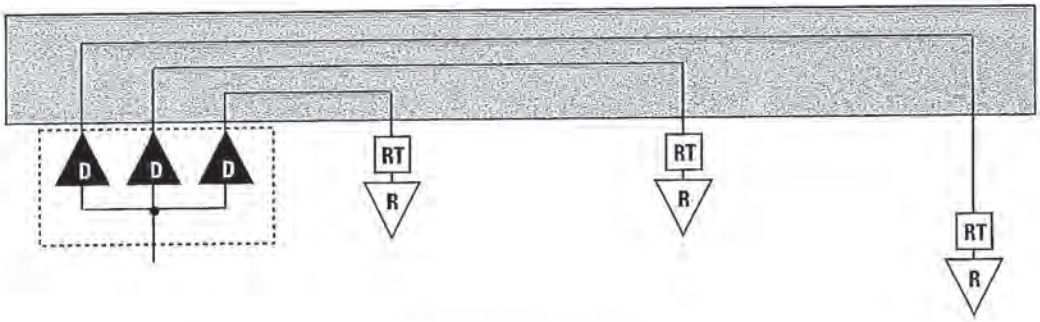


Multidrop Application with Double Termination

Again, this architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces). The advantages and disadvantages are the same as those discussed in 6.1.1.

6.1.3 Data Distribution with Point-to-Point Links

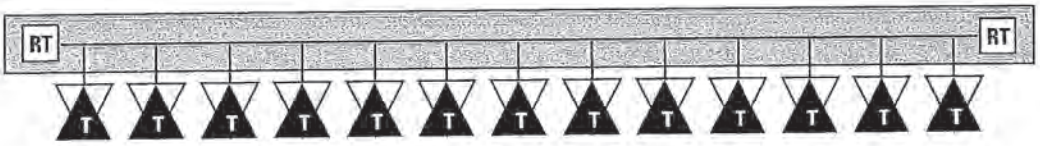
A distribution amplifier can also be used to buffer the signal into multiple copies which then drive independent interconnects to their loads. This offers optimized signal quality, the capability to drive long leads (long stub) to the loads, at the expense of interconnect density.



Data Distribution Application

6.1.4 Multipoint

The multipoint bus requires the least amount of interconnect (routing channels & connector pins), while providing bi-directional, half-duplex communication.



Multipoint Application

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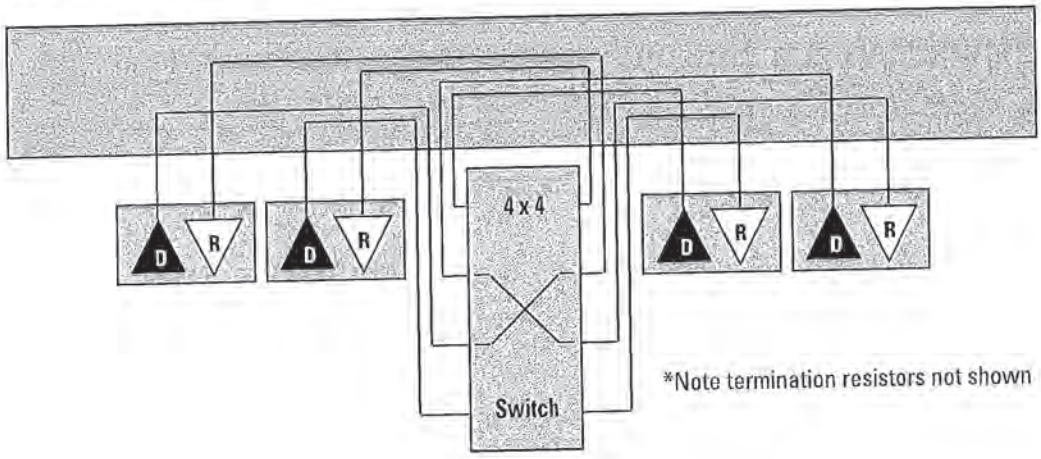
However, on this type of bus, there can only be one transaction at a time. Thus, a priority and arbitration scheme are typically required. These may be protocol or hardware solutions, depending upon the application.

6.1.4 Switch Matrix

Switch busses are growing in popularity for systems that require the very highest throughput possible. It is possible to have simultaneous transactions occurring on the switch bus at the same time and it has the cleanest electrical signal path of all the bus options (multidrop and multipoint, due to the no-stub effect).

The disadvantage of this type of scheme is that interconnect density increases with the number of loads, and also the complexity of the central switching card.

The switch application, due to its inherent optimized signal quality, is commonly used for links running hundreds of megabits per second into the Gigabit per second range. The top speed tends to be limited by the bandwidth of the interconnect.



Switch Application

6.2.0 BUS LVDS

6.2.1 System Benefits of Bus LVDS

There are numerous system benefits to using Bus LVDS over other technologies that have historically been used for bus interconnect. Many of these advantages are discussed next, but can be summed up with "Gigabits @ milliwatts!"

6.2.2 High-Speed Capability

Bus LVDS is capable of driving a multidrop or multipoint bus at high-speeds – for example:

- at 155Mbps across a 20 slot multipoint FR4 backplane
- at 400Mbps across a 10 slot multidrop FR4 backplane
- at 66MHz with ultra-low skew clock buffers
- at 800Mbps for point-to-point links

Previously, this has only really been achievable with the more costly high-speed ECL products. These present a translation challenge between common TTL devices and ECL drivers, and also power supply/termination problems. Other single-ended technologies were limited to sub 100MHz applications and presented tough termination and power dissipation problems. For a detailed comparison of back-plane technologies, please refer to *National Application note # 1123 – Sorting out Backplane Driver Alphabet Soup.*

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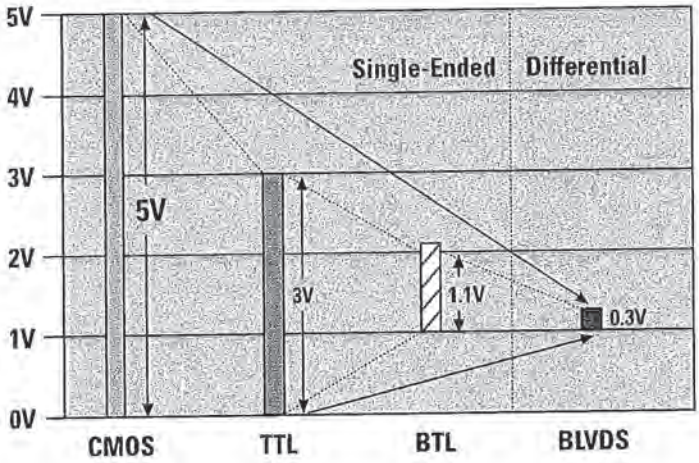
6.2.3 Low Power

Bus LVDS switches an interconnect with only 10mA of loop current. This is much less than other high performance bus technologies that use large amounts of current (as much as 80mA in the case of BTL and 40+mA for GTL) to switch a bus with an incident wave. Typically, the load power for Bus LVDS is only 2.5mW. The current-mode drivers tend to offer low power dissipation, even at high data signaling rates. Lastly, with the low swings required, the supply rails may be less than 5V, 3.3V or even 2.5V. These three reasons make LVDS and Bus LVDS components extremely low power.

6.2.4 Low Swing/Low Noise/Low EMI

Bus LVDS uses a low swing differential signal. This small balanced signal transition generates small EMI, and the current-mode driver limits spiking into the supply rails. These reasons make the LVDS driver capable of running at better than 10x the frequency of TTL at lower EMI levels.



Comparison of Voltage Swings for Various Backplane Technologies

CMOS and TTL technologies use a large swing and often large currents in order to switch a bus. This switching can cause ringing and undershoot which can be a large contributor to system EMI.

BTL addressed this noise issue by reducing its output swing to just 1V. However, it still uses large amounts of current to switch the bus with an incident wave (80mA typical) and still uses the single-ended approach with limited noise margins and a complex termination scheme.

As we have seen, Bus LVDS uses only 10mA to switch the bus with an incident wave, is low swing (300mV typical) and is differential. We saw in Section 4.3.2 how differential signaling can help substantially reduce system EMI. The small swing also provides the high-speed capability while consuming minimal power.

6.2.5 Low System Cost

All of National's Bus LVDS products are implemented in a core CMOS technology which allows for low manufacturing cost and the ability to integrate more functionality onto one piece of silicon. By putting the coding, clock recovery, and other PHY/LINK layer digital functions into the interface device, ASIC complexity and risk is greatly reduced. Immense system savings can be obtained through the use of the Serializer and Deserializer chipsets. Connectors, cable size and cost may be reduced. In most cases, these savings more than compensate for the interface silicon cost!

6.2.6 System Benefits

Besides the cost effectiveness of using Bus LVDS, there are also other system savings in using Bus LVDS:

- **Low Power**
  - Its CMOS design helps reduce the cost of system power supplies and cooling, enabling fan-free applications!
- **Simple Passive Terminations**
  - A bus can be implemented using only discrete components for termination. Other high-speed bus technologies such at GTL, BTL and ECL require active termination devices and/or odd ball supply rails (+1.5V, +2.1V for example) which add to system cost and power distribution complexity.
- **Serialization**
  - National's Bus LVDS portfolio consists of bus-able serializers and deserializers which reduce system interconnect and connector size.
- **Low Noise**
  - The low noise characteristic of Bus LVDS help with the limitation of EMI within a system which can help with system cycle times and system cost reductions.

6.3.0 BACKPLANE DESIGN CONSIDERATIONS

Prior to the start of any system design, the following methodology should be used.

1. System design starts with a solid power and ground distribution system. When this is left to the last step, it tends to be the source of noise and EMI problems.
2. Next, consider the transmission line configuration and layout. Optimize paths to provide the best signal quality. Locating certain devices close to the connector location and other devices (potential noise sources) far away is one way to do this. Give priority to the layout of the transmission line traces to avoid unnecessary via and in-balances.
3. Complete the remaining digital design.
4. Always review the completed layout.

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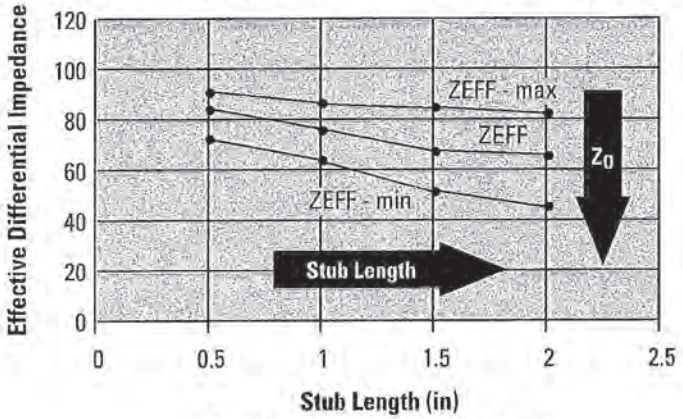
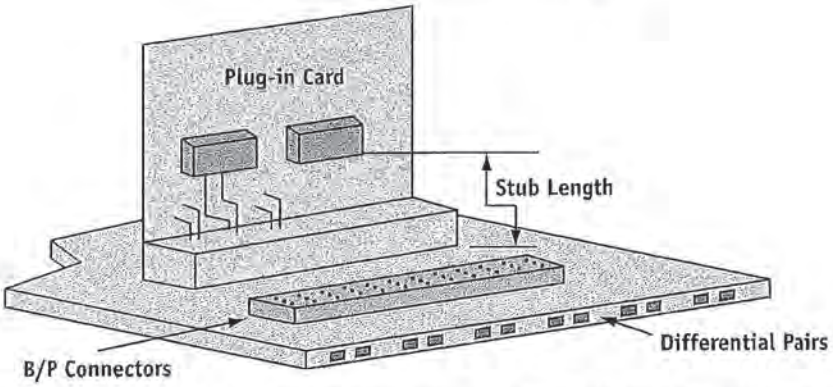
6.3.1 Loading Effects

The next figure shows the differential bus with one card plugged in. The card adds a load to the bus which is mainly composed of a bulk capacitance load (CD) resulting from the connector (2-3pF), the PCB trace (2-3pF) and the device (4-5pF), for a total load of about 10pF. Limit the number of vias on the card's stub to minimize capacitance loading. Also, keep stub lengths as short as possible. These two tips will help to maintain a high "loaded" bus impedance that will increase noise margins.

The TDR Simulated Differential Impedance of 20 Slot, Full Loaded BLVDS Backplane with Differential Z_0 = 130Ω



Source: NESA BLVDS WhitePaper



BLVDS is capable of operating in wild card configurations! Depending upon system noise margin goals, full card loading is NOT required. Termination selection is a bit tricky, but should be matched to a fully loaded case (or slightly higher). Waveshape is good even for half loaded or section loaded busses! Single-ended technologies can not support this feature due to noise margin violations.

The next figure provides a TDR simulation of a backplane impedance vs. loading.

- Case A shows the raw traces only (no via)
- Case B inserts the backplane connectors
- Case C adds all the cards into the bus, note that the cards do not include the device
- Case D adds the device to the card, thus it is a fully loaded system

Notice that about 50% of the loading is due only to the backplane connectors and their vias. Also notice how the velocity of the signal is slowed by the loading. This final value is equal to the parallel loading of the two 56Ω termination resistors.

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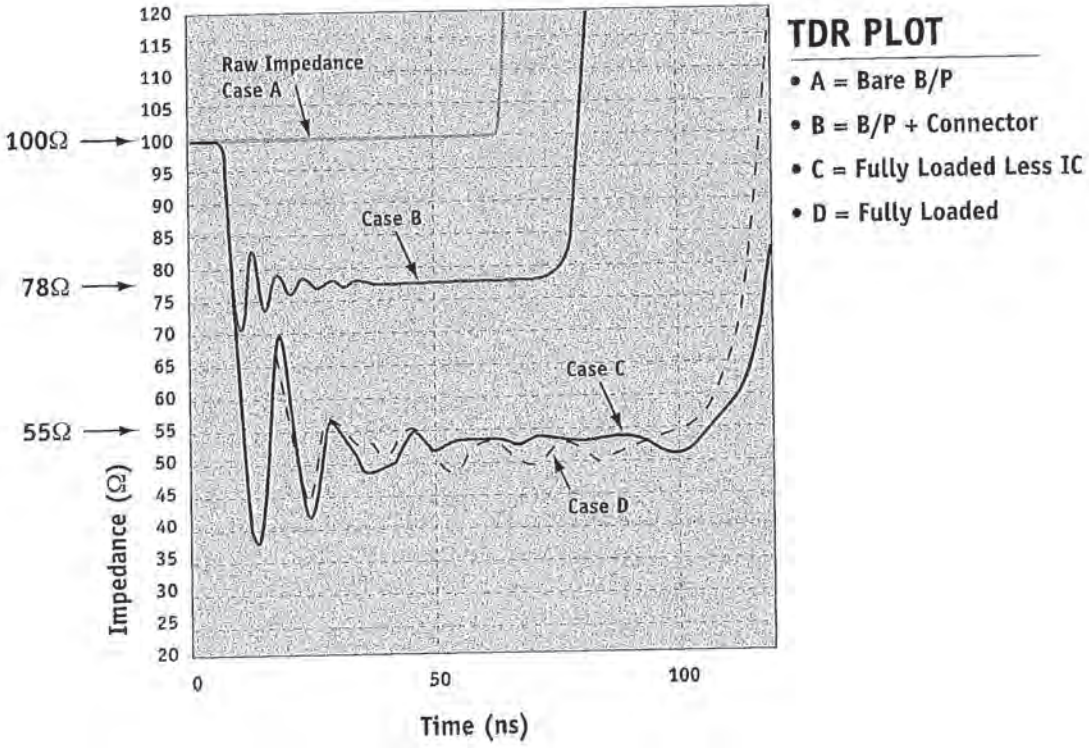

6.3.2 Bus Termination

Termination is required for two reasons:

1. Current-mode drivers require the resistor to complete the current loop.
2. BLVDS edge rates are fast and the interconnect will act as a transmission line, therefore terminations are needed to limit reflections.

BLVDS only requires a simple termination of a single surface mount resistor across the line at each end of the bus for multipoint applications. There is no need for a special V_T rail or active termination devices, as with single-ended technologies (TTL/BTL/GTL). The resistor should be equal to or slightly greater than the loaded differential impedance of the line. Typically, it is located at both ends of the backplane depending upon the configuration/application. (See also 6.3.5 on Failsafe Biasing).

6.3.3 Stub Length

Stubs - one golden rule: **The shorter the better!**

A long stub adds to the capacitive load, lowers the loaded impedance even more and tends to impact signal quality. For this reason, stub interconnect should be a microstrip and the number of vias (0-1 is best) should be limited. The graph below is from the NESA White Paper on BLVDS (available from www.national.com/appinfo/lvds/) and illustrates how increasing stub length lowers the loaded impedance. Stub length should be typically 1-1.5" or less.

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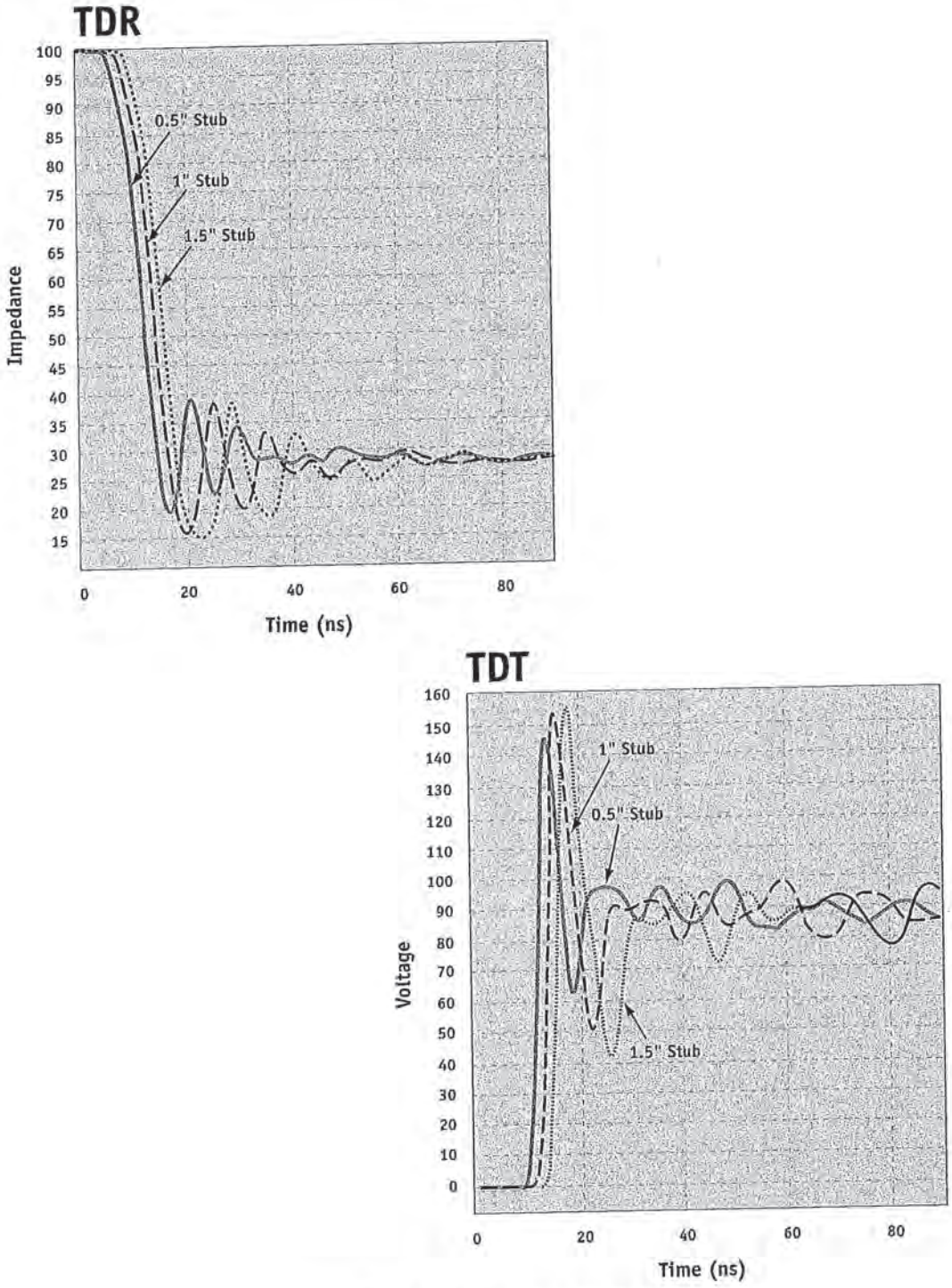

300ps Input Signal vs 0.5"/1.0"1.5" Stub

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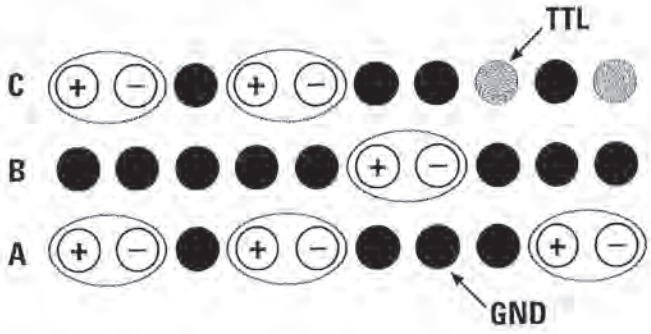
6.3.4 Connectors

Connectors are a complex topic and are the subject of many heated debates at standard committee meetings. There are two basic types: standard matrix based connectors (3 rows of 32-pins) and special connectors. The special connectors may be optimized for differential signals or may use elaborate techniques to clamp to the PCB. The elaborate connectors tend to avoid via structures and thus offer the highest bandwidth. They are also very application specific and tend to be rather expensive.

More common is the use of standard connectors for a mix of differential, power, ground and single-ended connections (see below). The graphic below shows a variety of pinout recommendations for single-ended and differential options.



Typical Connector Pinouts

For differential lines in a matrix (single-ended) connector, adjacent pins in a row tend to be better as the electrical length are the same. The row with the shorter path provides a better path over the longer row also.

Ground signal assignment can be used to isolate large swing (TTL) signals from the small-swing lines as shown above.

Connector Example: Teradyne VHDM High-Speed Differential Connector

This is a differentially optimized high-density connector for applications into the Gigabit per second range. It is offered in both an 8 row (which provides 3 differential pairs) and a 5 row (which provides 2 differential pairs) configurations. The 8 row connector can coexist with the basic 8 row VHDM single-ended connector and also power/ground contacts. Shielding is provided between wafers providing excellent isolation of signal contacts. The backplane layout is also improved over earlier generations and the new footprint now supports wider traces (10mils) to be routed through the pin field easing backplane design. The backplane side of the connector accepts either the single-ended or differential versions of VHDM. Skew has been minimized within the pair and also the pairs are routed together (see next drawing). This is an example of a high-throughput differential optimized connector that provides excellent signal quality. For details, please visit the Teradyne website at:
www.teradyne.com/prods/bps/vhdm/hsd.html

Testing is planned at National for the Summer of 2000 to evaluate this connector with various LVDS devices. Check our LVDS website for the results of this testing to be available late Summer 2000.

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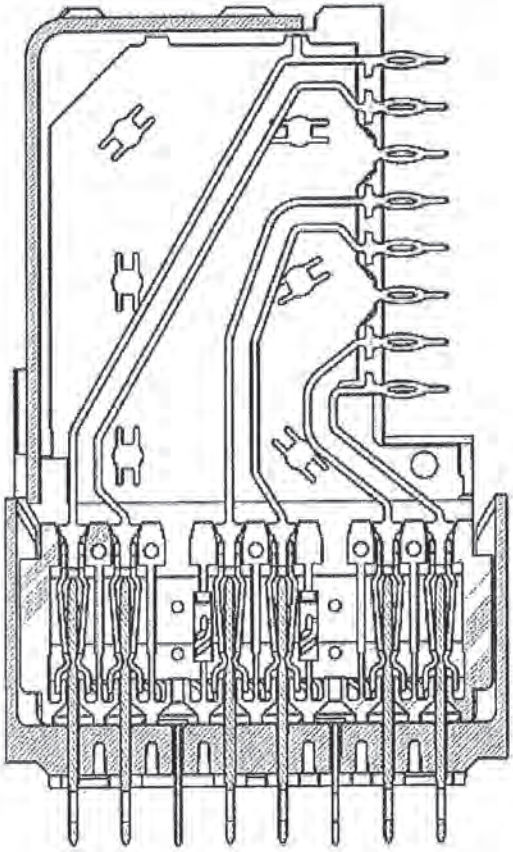

Cross Section of VHDM HSD
(Graphic courtesy of Teradyne)

6.3.5 Failsafe Biasing

Failsafe biasing may be required if a known state is required on the bus when any of the following conditions occur:

- All drivers are in TRI-STATE® – common in multipoint applications.
- All drivers are removed or powered-off

If this is the case, additional biasing (beyond the internal failsafe biasing of the receivers) may be provided with a failsafe biasing (power) termination as shown in the next figure.

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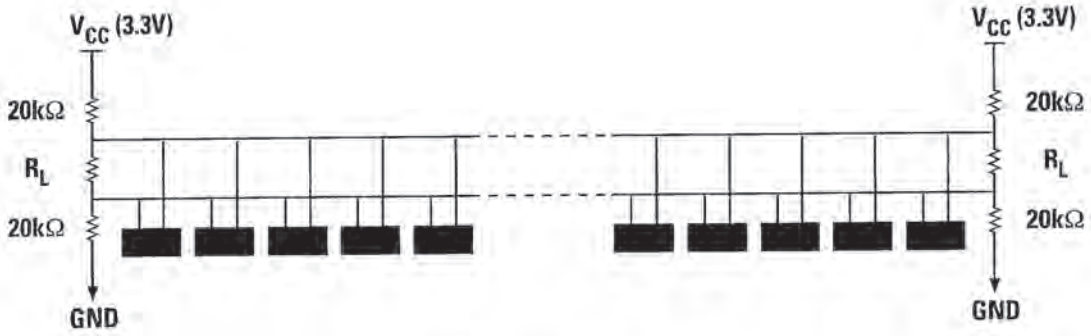

Multipoint Bus with Failsafe Bias

In selecting failsafe resistor values note the following:

- The magnitude of the resistors should be 1 to 2 orders higher than the termination resistor, to prevent excessive loading to the driver and waveform distortion
- The mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common-mode shift from occurring between active and TRI-STATE® (passive) bus conditions
- The pull-up and pull-down resistors should be used at both ends of the bus for quickest response
- Note that signal quality is reduced as compared to active driving (on/on)
- See Chapter 4 for equations for selecting failsafe biasing resistors

6.3.6 Hot Plugging/Live Insertion

Live Insertion, or Hot Swapping, is of particular importance to the telecommunications marketplace. In these applications, it is critical that maintenance, upgrading and repair can be performed without shutting down the entire system or causing disruption to the traffic on the backplane. BLVDS's wide common-mode range of ±1V plays a key role in supporting this function. Upon insertion of a card into a live backplane, the occurrence of abnormalities on the signals are common on both signals, thus data is not impacted. This allows for safe hot swapping of cards, making the systems robust and reliable.

Lab testing done in the National LVDS Interface Lab has shown zero-bit errors while plugging in or removing cards from an active bus (BERT test). During the test, up to four cards were inserted at once without an error! This is due to the fact that the differential lines equally load the active line on contact and any glitch seen is a common-mode modulation that is ignored by the receivers.

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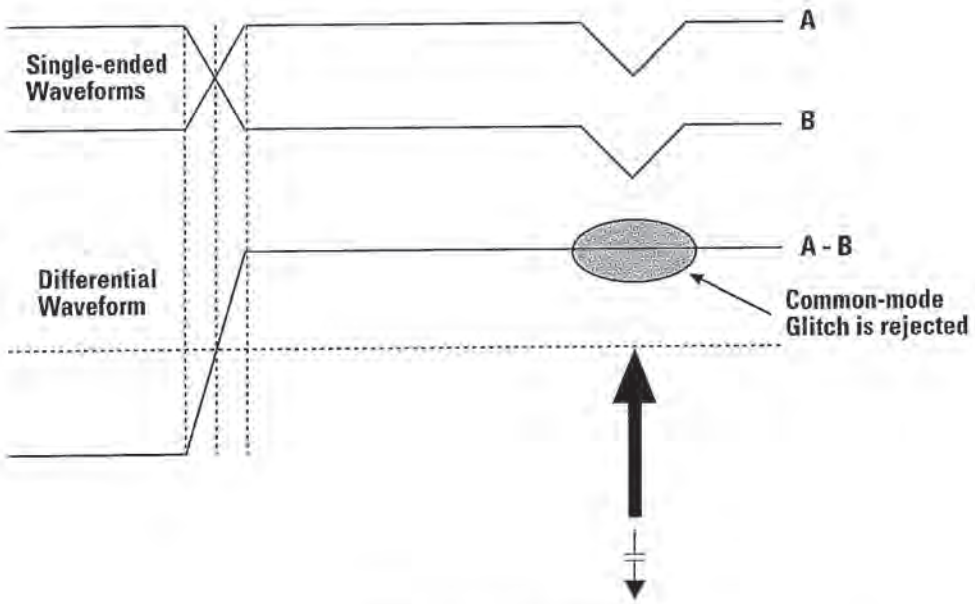

Live Insertion Waveforms

However, standard power sequencing is still recommended to ensure proper biasing of the devices (substrate). For insertion, the following sequence should be guaranteed by hardware design:

1. Ground
2. Power
3. I/O pins

For removal, the reverse order is recommended (3-2-1). This sequence can be supported a number of ways. Staggered power pin connectors may be employed (available from multiple sources and even compatible with many matrix connector styles). Multiple connectors are also commonly used. A D_{IN} connector for the I/O, and "Jack" like connectors for power and ground is one approach. Yet another option uses card edge contact on the rails to establish a GND bias when the card is first inserted into the card rail.

6.4.0 ADDITIONAL INFORMATION

Detailed backplane design information is available from our website in the form of white papers and also application notes. National has also teamed up with NESA (North East System Associates Inc.) and jointly published a number of white papers and conference papers. Recent papers are available from both websites:

www.national.com/appinfo/lvds/

www.nesa.com

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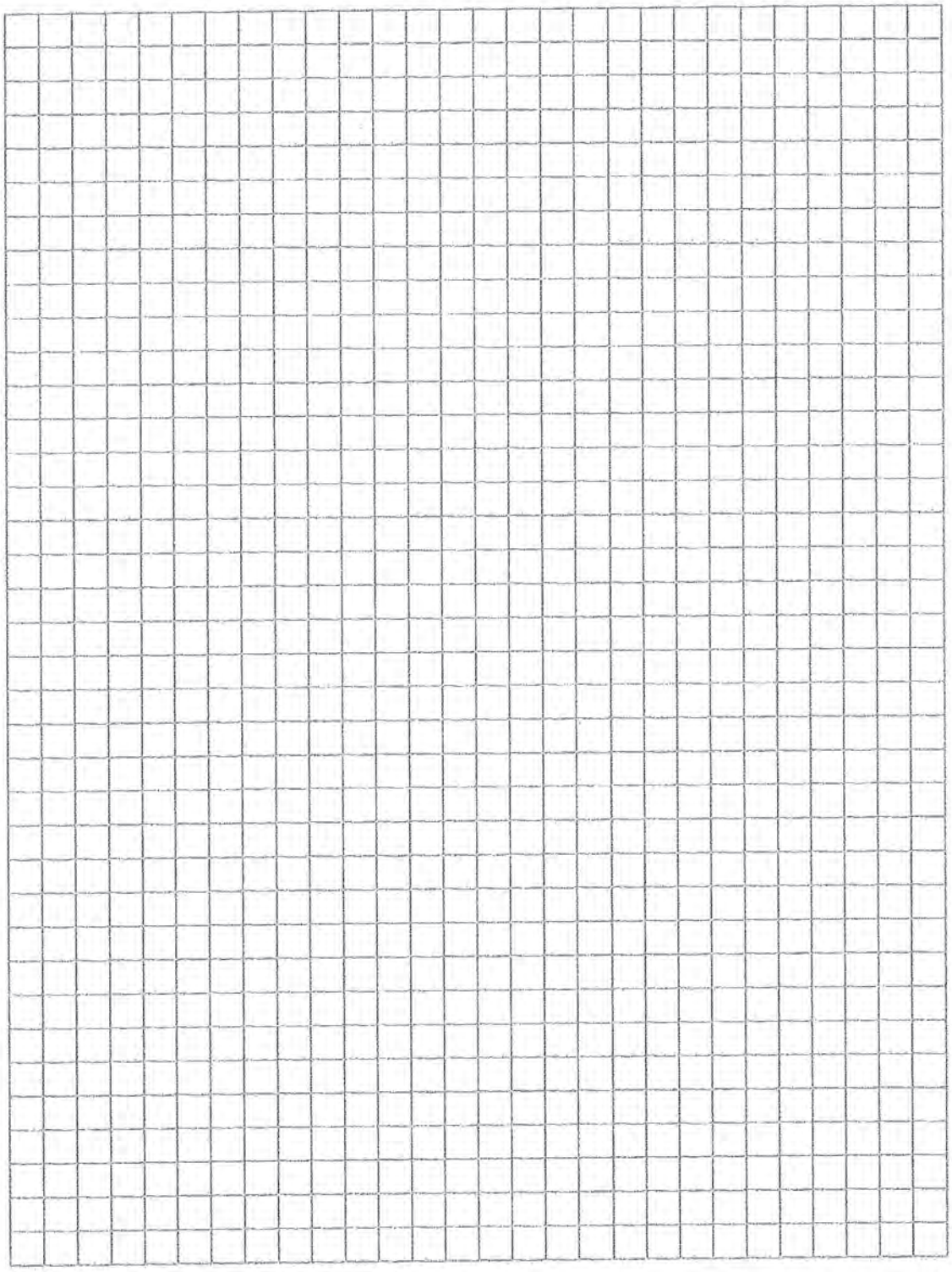
NOTES



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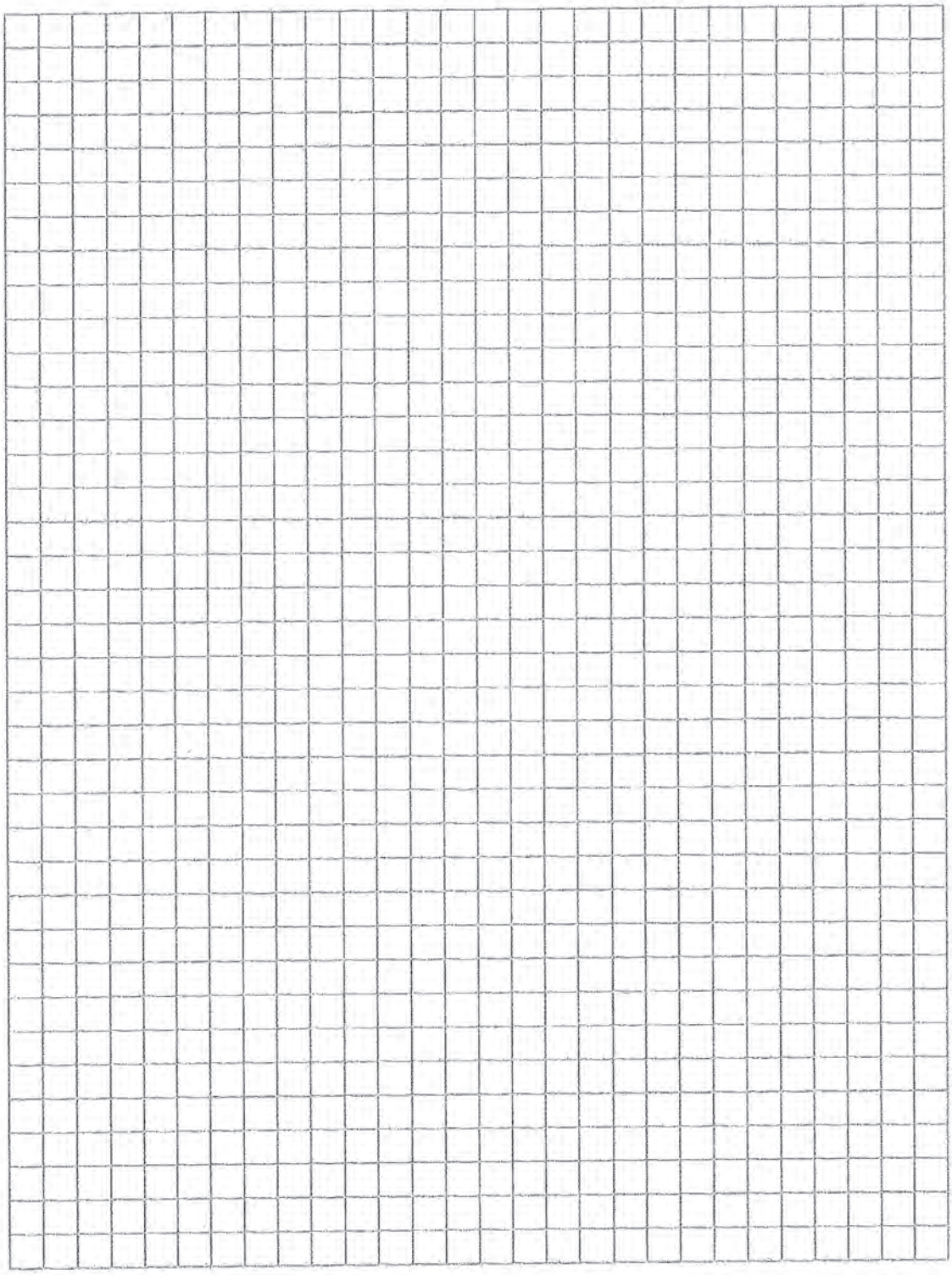

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LVDS Evaluation Kits

Chapter 7

7.0.0 LVDS EVALUATION BOARDS AND EVALUATION KITS

Evaluation kits, offered at a nominal cost, demonstrate the LVDS Physical Layer Interface devices. Please consult the LVDS website for a link to the page that provides updated information on the Evaluation Kits. The "Evaluation/Demo Board" page contains:

- LVDS Family (LVDS, Channel Link, Bus LVDS, etc)
- A short description of the board or kit
- A list of the NSID(s) (part numbers) that are on the PCBs
- The kit's order number (Order Number)
- An update/revision/errata link (if applicable)

Also note that on selected kits, the user's manual for the specific kit can now be downloaded directly from this page. This allows the user to determine exactly the content, capability, and features of the kit prior to purchasing the kit.

7.1.0 LVDS KITS - SHORT DESCRIPTIONS

7.1.1 The Generic LVDS Evaluation Boards

The Generic LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over PCB trace, twisted pair cable, or custom transmission medium. Flow through LVDS quad drivers and receivers are used on the board. They can represent the LVDS I/O characteristics of most of National's 3.3V LVDS devices. Included in the latter part of this section is the complete user's documentation for the new LVDS47/48EVK. See Section 7.2.0 below.

While supplies last, the original generic LVDS evaluation board is available as both an assembled kit (LVDSEVAL-001) and also as an un-stuffed PCB (order as a literature piece, LIT# 550061-001). This PCB accommodates a SCSI-2 50 pin cable interface.

7.1.2 Channel Link Evaluation Kits

These boards are fully populated. TTL signals are accessed through IDC connectors on the transmitter and receiver boards. The boards are interconnected via a ribbon cable that can be modified for custom lengths for the 21 & 28-bit chipsets. The 48-bit chipset features a 3M MDR cable and connector system. These evaluation boards are useful for analyzing the operation of National's high-speed Channel Link devices.

7.1.3 Bus LVDS Evaluation Kits

These boards are fully populated. Currently a mini backplane kit is offered (different RX device options available). A stand-alone test system is also offered. The BLVDS03 kit provides a PRBS generator that provides data to the BLVDS Serializer and also checks the received data from the BLVDS Deserializer. This kit only requires a power supply voltage. These evaluation boards are useful for analyzing the operation of National's New Bus LVDS SER/DES devices.

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7.1.4 Special Function LVDS Evaluation Kits

New special function LVDS/BLVDS devices are being developed for special applications. The first EVAL KIT is for the DS90CP22 2x2 800Mbps Digital Crosspoint Switch. Check our website for the latest information on new kits.

7.1.5 FPD-Link Evaluation Kits

These boards are fully populated. TTL signals are accessed through IDC connectors on the transmitter and receiver boards. The boards are interconnected via a cable. These evaluation boards are useful for analyzing the operation of National's high-speed FPD-Link and LDI devices. Current information on the FPD Link Evaluation Kits can be accessed from the FPD website at: **www.national.com/appinfo/fpd/**

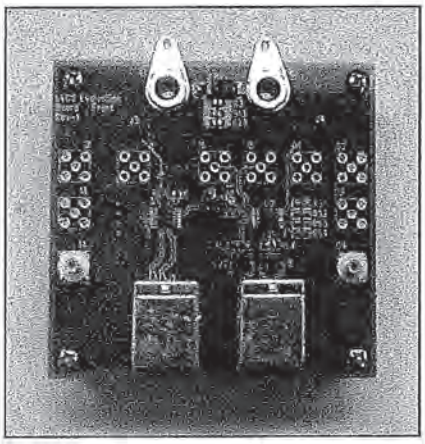
7.1.5 Related Parts

- Use the DS90C031/032 on the original generic LVDS evaluation board (LVDSEVAL-001) to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.
- Use the DS90LV047A/048A on the new generic LVDS evaluation board (LVDS47/48EVK) to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices.

The remainder of this chapter explains the operation of the new generic LVDS Evaluation Board.

7.2.0 THE GENERIC LVDS EVALUATION KIT – THE LVDS4748EVK

7.2.1 The Flow Through LVDS Evaluation Board



The Flow Through LVDS Evaluation Board

The Flow Through LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over a PCB trace, RJ45 connector and CAT5 UTP cable, or custom transmission medium. Though LVDS quad drivers and receivers are used on the board, they can represent the standard LVDS I/O characteristics of most of National's LVDS devices. We can also use the DS90LV047A/048A to represent the LVDS I/O characteristics of 3V Channel Link and 3V FPD-Link devices.

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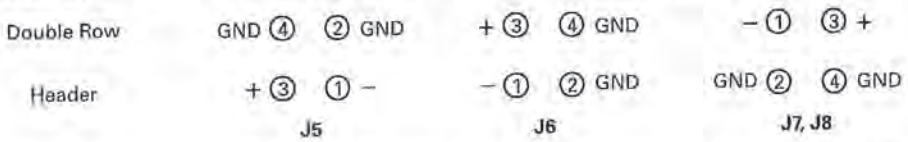
7.2.2 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of RJ45 cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation Kit is LVDS47/48EVK. In this application note, the following differential signal nomenclature has been used: "Jx-3" represents the true signal and "Jx-1" represents the inverting signal. On the PCB, the true signal is represented by a '+' and the inverting signal is on the adjacent header pin as shown below.



The two adjacent ground pins are there to view the true or inverting signal single-endedly. Input signals are represented with an "I" while receiver outputs are represented with an "O."

7.2.3 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately. The five test cases are shown in the following figure.

LVDS Channel #1A: LVDS Line Driver
This test channel provides test points for an isolated driver with a standard 100Ω differential termination load. Probe access for the driver outputs is provided at test points on J5-1 and J5-3. The driver input signal (I1) is terminated with a 50Ω termination resistor (RT1) on the bottom side of the PCB.

LVDS Channel #1B: LVDS Receiver
This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either two separate 50Ω terminations (RT5 and RT6) (each line to ground) or a 100Ω resistor connected across the inputs (differential). The first option allows for a standard signal generator interface. Input signals are connected at test points I5 (R_{IN-}) and I6 (R_{IN+}). A PCB option for a series 453Ω resistor (RS1) is also provided in case 50Ω probes are employed on the receiver output signal. The default setting is with two separate 50Ω terminations (RT5 and RT6) and without the series 453Ω resistor (RS1) for use of high impedance probes. The receiver output signal may be probed at test point O1.

LVDS Channel #2: PCB Interconnect
This test channel connects Driver #2 to Receiver #2 via a pure PCB interconnect. A test point interface of the LVDS signaling is provided at test point J6-1 and J6-3. The driver input signal (I2) is terminated with a 50Ω termination resistor (RT2) on the bottom side of the PCB. The receiver output signal may be probed at test point O2. A PCB option for a series 453Ω resistor (RS2) is also provided in case 50Ω probes are employed on the receiver output signal. The default setting is without the series 453Ω resistor for use of high impedance probes. A direct probe connection is possible with a TEK P6247 differential probe high impedance probe (>1GHz bandwidth) on the LVDS signals at test points J6-1 and J6-3. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel #3: Cable Interconnect
This test channel connects Driver #3 to Receiver #3 via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I3) is terminated with a 50Ω termination resistor (RT3) on the bottom side of the PCB. LVDS signals are probed via test points on J7. The receiver output signal may be probed at test point O3. A PCB option for a series 453Ω resistor (RS3) is also provided in case 50Ω probes are employed on the receiver output signal (see options section). The default setting is without the series 453Ω resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1GHz bandwidth) on the LVDS signals at test point J7-1 and J7-3.

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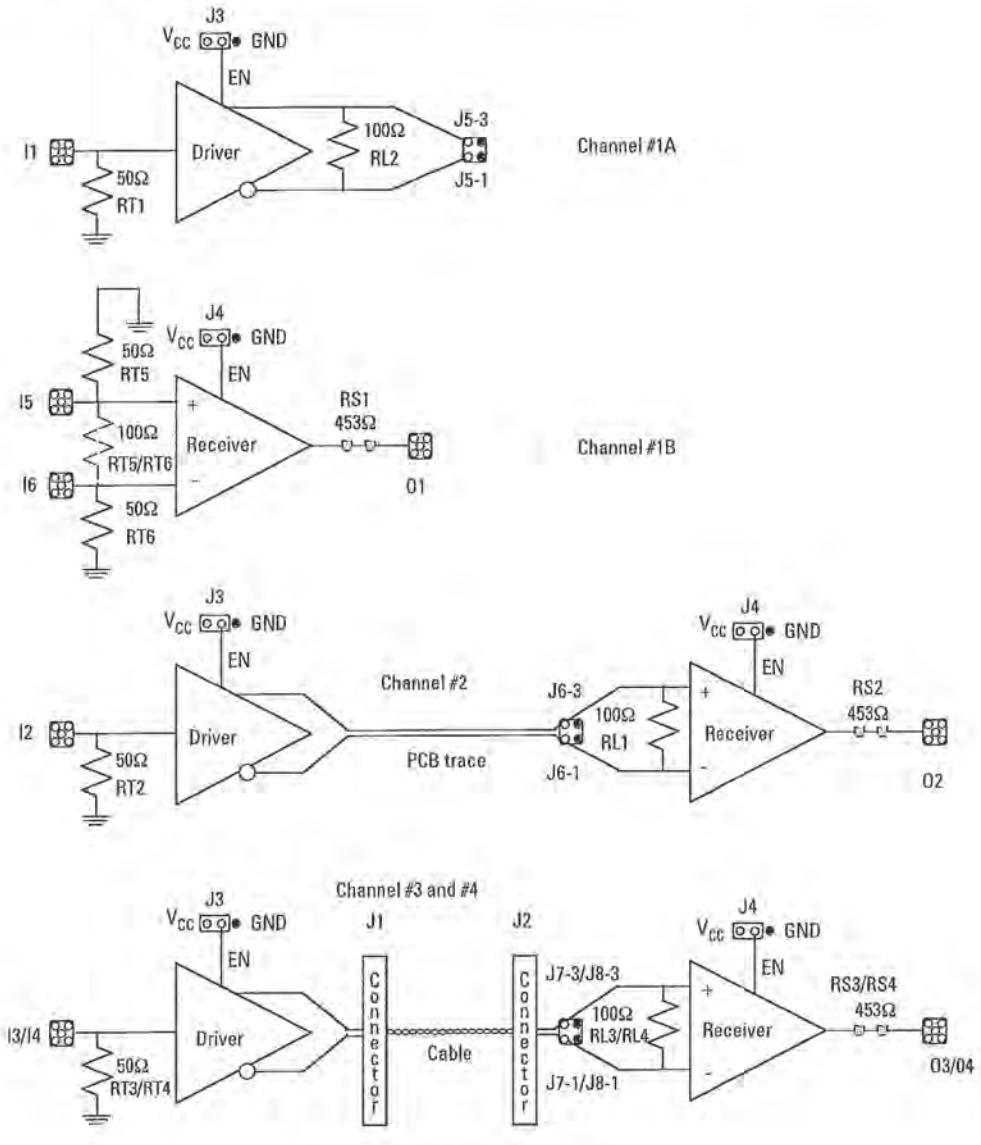
LVDS Channel #4: Cable Interconnect

This test channel connects Driver #4 to Receiver #4 also via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I4) is terminated with a 50Ω termination resistor (RT4) on the bottom side of the PCB. LVDS signals are probed via test points on J8. The receiver output signal may be probed at test point O4. A PCB option for a series 453Ω resistor (RS4) is also provided in case 50Ω probes are employed on the receiver output signal. The default setting is without the series 453Ω resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1 GHz bandwidth) on the LVDS signals at test point J8-1 and J8-3. This channel duplicates channel #3 so that it may be used for a clock function or for cable crosstalk measurements.



PCB Block Diagram

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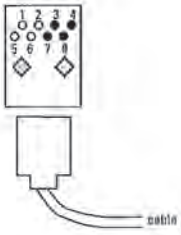
7.2.4 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a CAT 5 four twisted pair (8-pin) RJ45 cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the Ethernet standard and the cable is widely available. The connector is 8 position, with 0.10" centers and the pairs are pinned out up and down. For example, pair 1 is on pins 1 and 5, not pins 1 and 2 (see Figure below).

IMPORTANT NOTE: The 2 unused pairs are connected to ground. Other cables may also be used if they are built up.

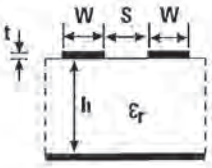


RJ45 Connector

7.2.5 PCB Design

Due to the high-speed switching rates obtainable by LVDS, a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal.

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, refer to PCB layout between U1 and J1). Employing differential traces will ensure a low emission design and maximum common-mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common-mode. Also, by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable's differential characteristic impedance). Equations for calculating differential impedance are contained in National application note AN-905 for both microstrip and stripline differential PCB traces.



For the microstrip line, the differential impedance, Z_{DIFF}, is:

$$Z_{DIFF} \cong 2Z_O\,(1 - 0.48e^{-0.96S/h})\Omega$$

For the new evaluation board h = 24mils, S = 11mils and Z_O = 70Ω. Calculating the differential impedance, Z_{DIFF}, is:

$$Z_{DIFF} \cong 2Z_O\,(1 - 0.48e^{-0.96(11/24)})\Omega$$

$$2\,(70)\,(0.69086)\Omega$$

$$96.72\Omega$$

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor mini-

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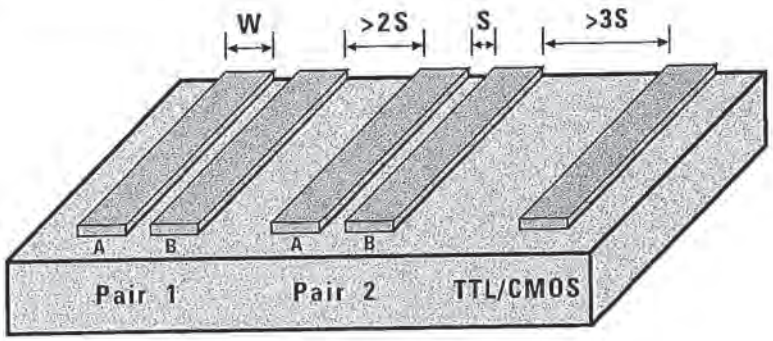
mizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match, the higher the signal fidelity and the less common-mode reflections will occur (lower emissions too). A typical value is 100Ω ±1%.

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

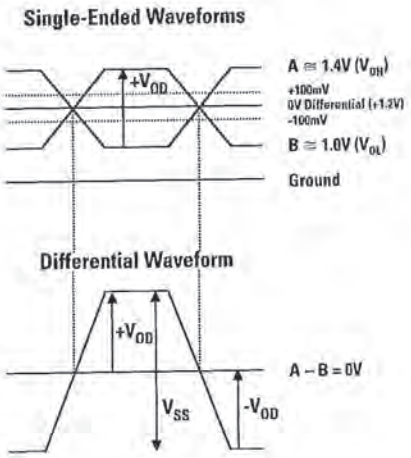


Pair Spacing for Differential Lines

Bypassing capacitors are recommended for each package. A 0.1 µF is sufficient on the quad driver or receiver device (CB1 and CB2) however, additional smaller value capacitors may be added (i.e. 0.001µF at CB21 and CB22) if desired. Traces connecting V_{CC} and ground should be wide (low impedance, not 50Ω dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB3, CB13, and CB23 if desired.

7.2.6 Sample Waveforms from the LVDS Evaluation PCB

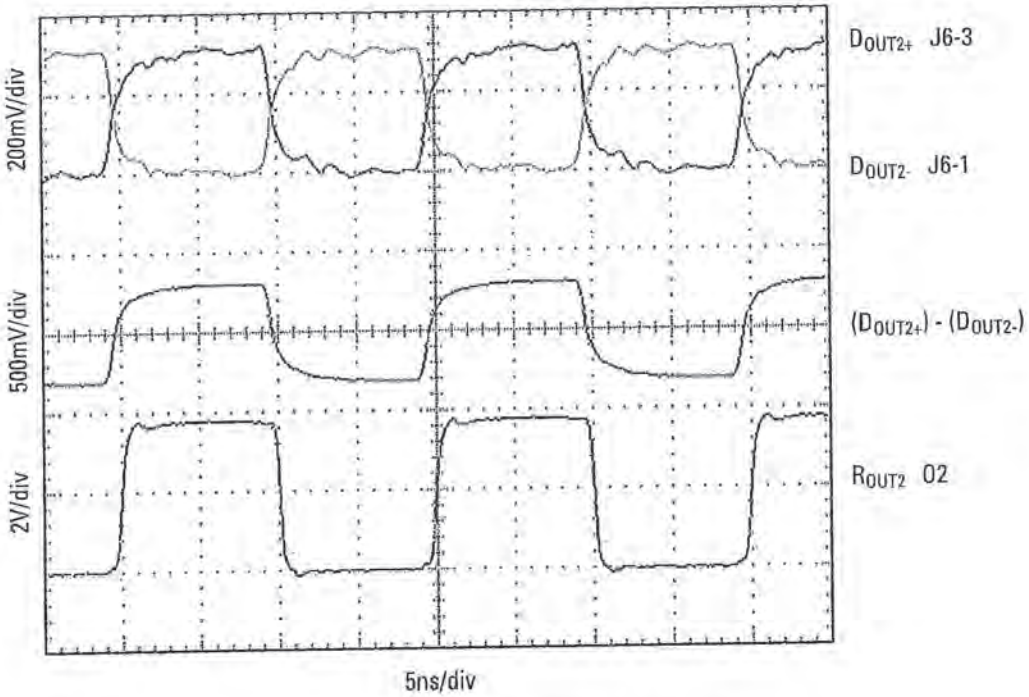
Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals have a V_{OD} specification of 250mV to 450mV with a typical V_{OS} of 1.2V. Our devices have a typical V_{OD} of 300mV, but for the example below, we will use a signal between 1.0 V (V_{OL}) and 1.4 V (V_{OH}) for a 400 mV V_{OD}. The differential waveform is constructed by subtracting the Jx-1 (inverting) signal from the Jx-3 (true) signal. V_{OD} = (Jx-3) – (Jx-1). The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in the following figure.



Single-Ended & Differential Waveforms

The PCB interconnect signal (LVDS Channel #2) can be measured at the receiver inputs (test points J6-1 and J6-3). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See figure below. Note that the data rate is 100Mbps and the differential waveform (V_{DIFF} = D_{OUT2+} - D_{OUT2-}) shows fast transition times with little distortion.

In the next four figures, the top two waveforms are the single-ended outputs (between the driver and receiver), the middle waveform is the calculated differential output signal from the two single-ended signals and the bottom waveform is the output TTL signal from the receiver.



LVDS Channel #2 Waveforms — PCB Interconnect

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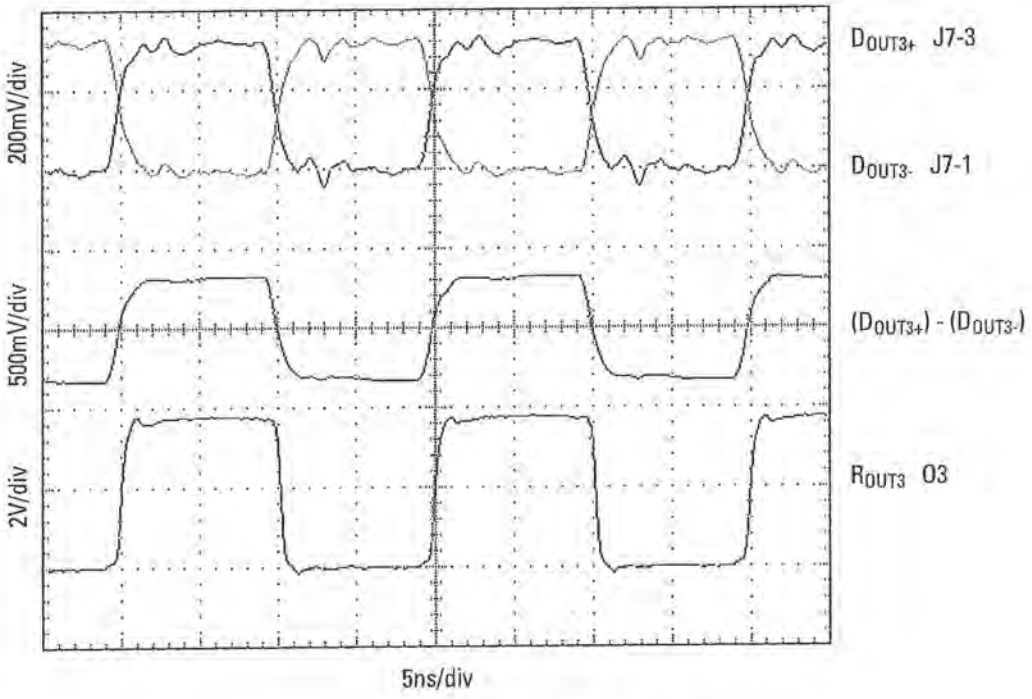
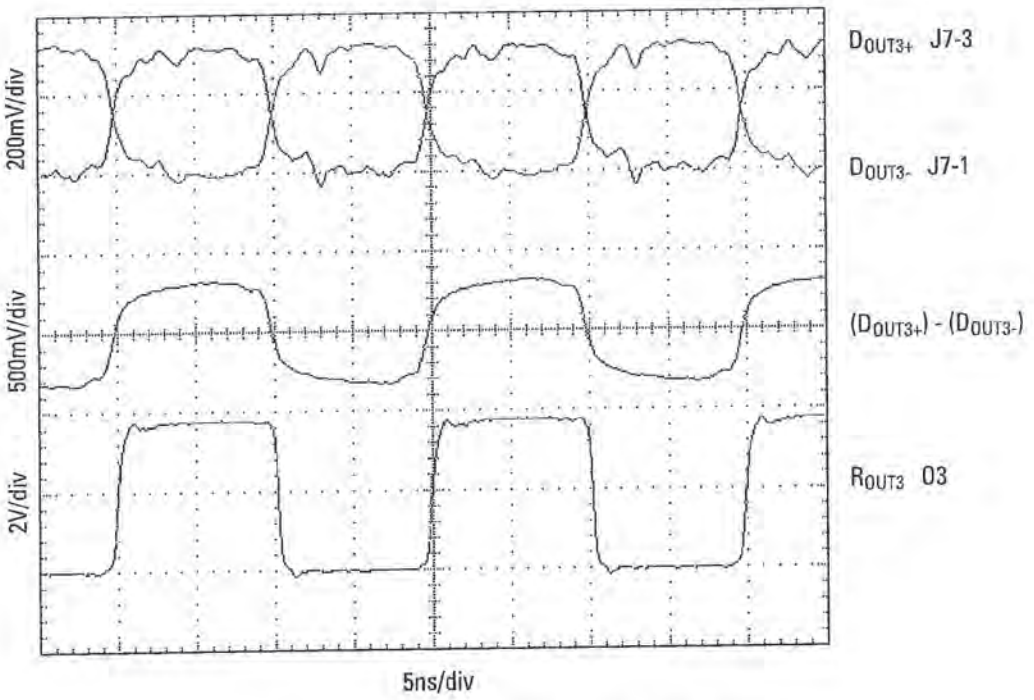
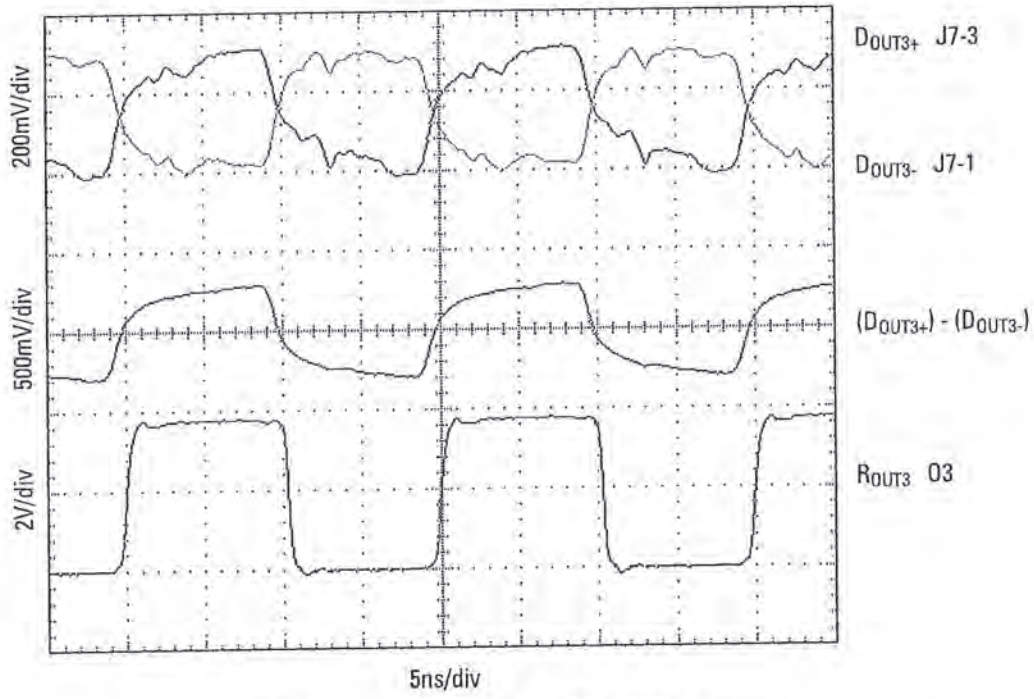
The cable interconnect signal is also measured at the receiver inputs (test points J7-1 & J7-3 and J8-1 & J8-3). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with an RJ45 cable of 1 meter, 5 meters and 10 meters in length are shown in the next three figures. Note the additional transition time slowing due to the cable's filter effects on the 5 meter and 10 meter test case.



LVDS Channel #3 Waveforms - 1m Cable Interconnect



LVDS Channel #3 Waveforms - 5m Cable Interconnect



LVDS Channel #3 Waveforms - 10m Cable Interconnect

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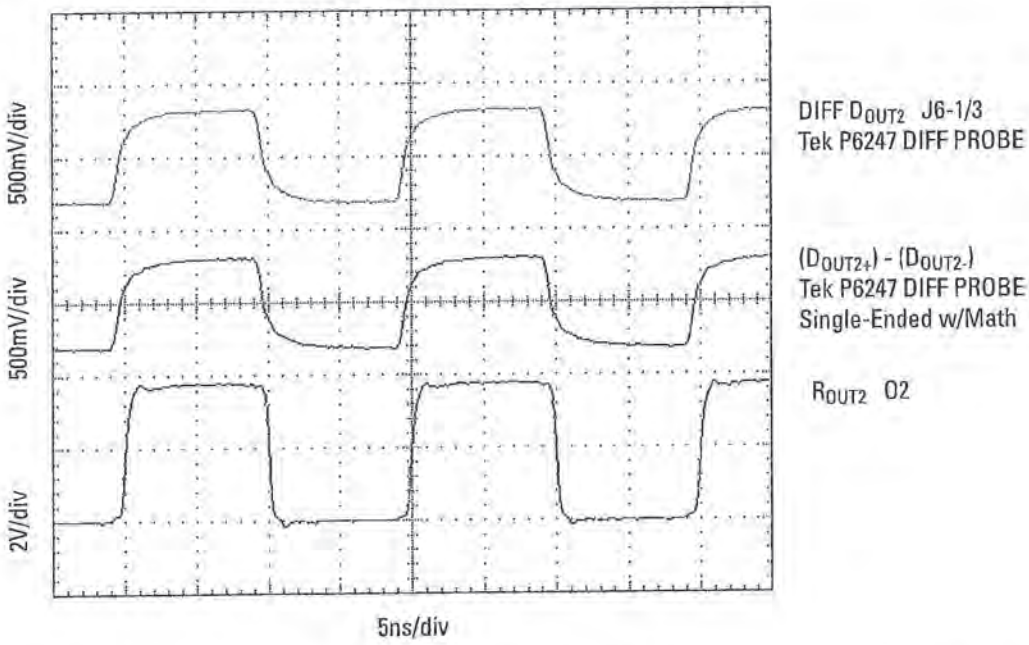
7.2.7 Probing of High-Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). Either a high impedance probe (100kΩ or greater) or the TEK P6247 differential probe (>1GHz bandwidth) must be used. The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 GHz (4 GHz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK TDS 684B Digital Real Time scope (>1GHz bandwidth) and TEK P6247 differential probe heads. These probes offer 200kΩ, 1pF loading and a bandwidth of 1GHz. This test equipment was used to acquire the waveforms shown.

The TEK P6247 differential probes may be used to measure the differential LVDS signal or each signal of the differential pair single-ended. This test equipment was used to acquire the waveforms differentially as well as single-endedly with the differential signal calculated by (DOUT+) – (DOUT-) shown in the figure below. You can see that both of the differential signals look identical. The method in which you acquire the single-ended signals is important (such as matching probe types and lengths) if you intend to calculate the differential signal from the two single-ended signals.



LVDS Channel #2 Waveforms - Differential and Calculated Differential from Single-Ended Waveform

LVDS waveforms may also be measured with high impedance probes such as common SD14 probe heads. These probes offer 100kΩ, 0.4pF loading and a bandwidth of 4 GHz. These probes connect to a TEK 11801B scope (50 GHz bandwidth). Probes with standard 50Ω loading should not be used on LVDS lines since they will load them too heavily. 50Ω probes may be used on the receiver output signal in conjunction with the 453Ω series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50Ω/(450Ω + 50Ω) or 1/10) of the output signal and the receiver output is loaded with 500Ω to ground.

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7.2.8 Demo PCB Options

Option 1: 453Ω Resistors
A provision for a series 453Ω resistor (RS1, RS2, RS3 and RS4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 453Ω resistor, a standard 50Ω scope probe may be used (500Ω total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver
The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J3). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the driver, connect the jumper to the power plane, to disable the driver connect the jumper to the ground.

Option 3: Disabling the LVDS Receiver
The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J4). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the receiver, connect the jumper to the power plane, to disable the receiver connect the jumper to ground.

Option 4: Cables
Different cables may also be tested (different lengths, materials, constructions). A standard RJ45 8-pin connector/pinout has been used (J1 and J2). Simply plug in the RJ45 1 meter or 5 meter cables included in the kit or build a custom cable.

Option 5: SMA or SMB Connectors
Both SMA and SMB connectors will fit the footprint on the boards for the driver inputs I1-4, receiver outputs O1-4 and the single receiver inputs I5-6. The board is loaded with SMBs on I4 and O4.

Option 6: Receiver Termination (Channel #1B)
The separate receiver input signals can be terminated separately (50Ω on each line to ground) utilizing pads RT5 (inverting to ground) and RT6 (true input to ground) for a signal generator interface. In addition, a single 100Ω differential resistor (across pads RT5 and RT6) can be used if the device is to be driven by a differential driver. Be sure to remove the 50Ω termination resistors RT5 and RT6 if you plan to use the 100Ω differential resistor.

7.2.9 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1. Connect signal common (Ground) to the pierced lug terminal marked GND
2. Connect the power supply lead to the pierced lug terminal marked V_{CC} (3.3V)
3. Set J3 & J4 jumpers to the power plane ("ON") to enable the drivers and receivers
4. Connect enclosed RJ45 cable between connectors J1 and J2
5. Connect a signal generator to the driver input (I4) with:
   a) frequency = 50 MHz (100 Mbps)
   b) V_{IL} = 0V & V_{IH} = 3.0V
   c) t_r & t_f = 2 ns
   d) duty cycle = 50% (square wave)
6. Connect differential probes to test points J8-1 and J8-3
7. View LVDS signals using the same voltage offset and volts/div settings on the scope with the TEK P6247 differential probes. View the output signal on a separate channel from test point O4. The signals that you will see should resemble the LVDS Channel #3 Waveform - 1m or 5m Cable Interconnect figure.

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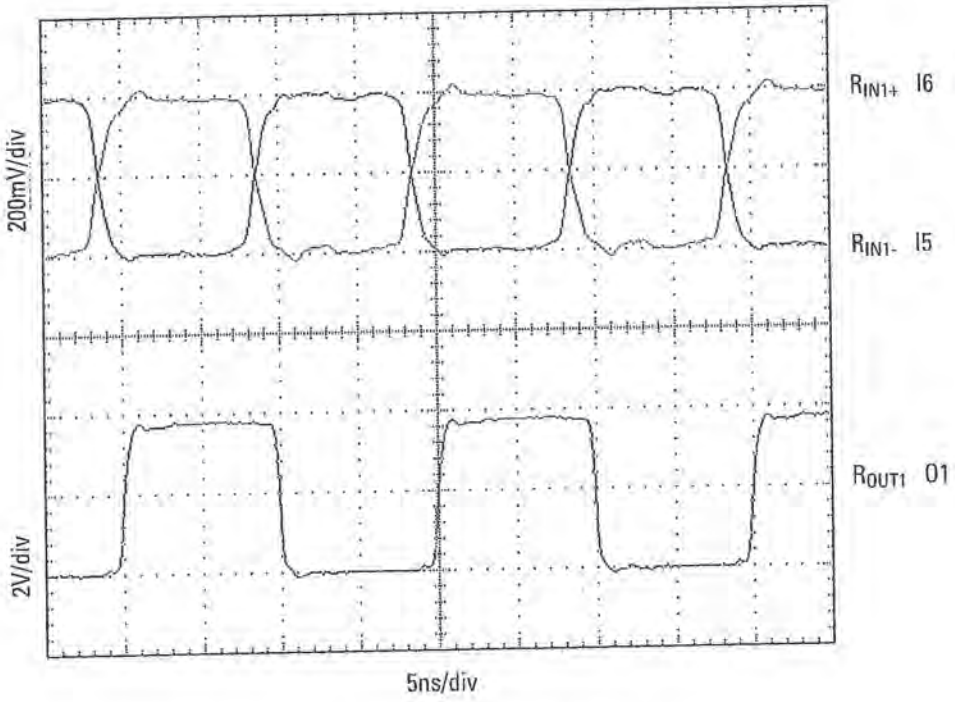
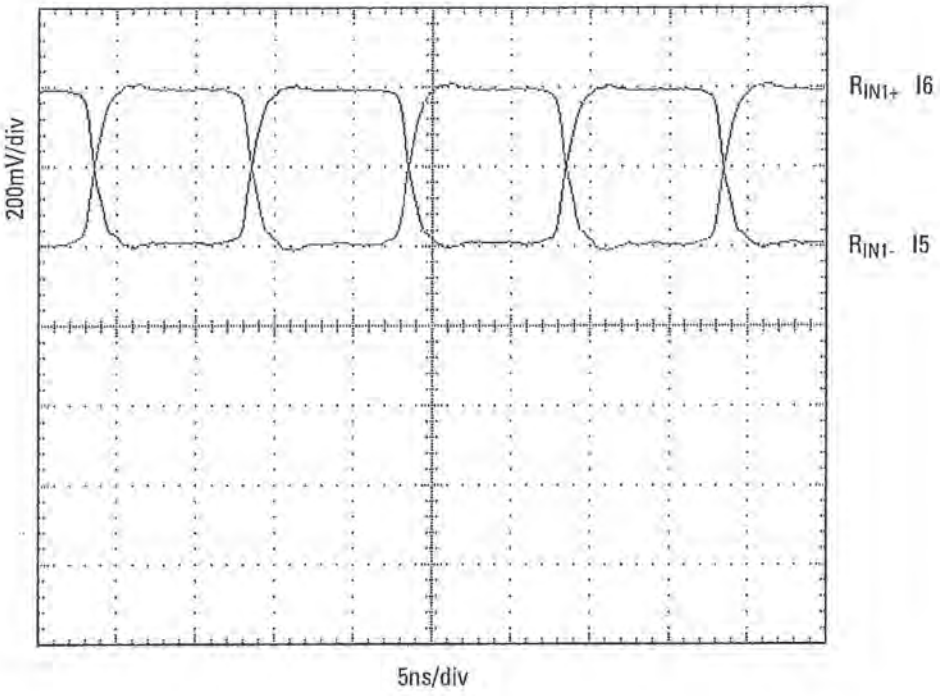
7.2.10 Common-Mode Noise

When the receiver (DS90LV048A) is enabled, a small amount of common-mode noise is passed from the output of the receiver to the inputs as shown in the next figure. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. A design improvement was made to the DS90LV048A to reduce the magnitude of the noise coupled back to the inputs, reducing the feedback by 30% compared to prior devices. This noise will not be observed if the receiver device is disabled by setting J4 to "OFF" as shown in the following figure.



LVDS Channel #1B Waveforms
A Small Amount of Common-Mode Noise Coupled from Output to Input



LVDS Channel #1B Waveforms – Output Disabled

7.2.11 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for high-speed data transmission applications.

7.2.12 Appendix

Typical test equipment used for LVDS measurements:

Signal Generator	TEK HFS 9009
Oscilloscope	TEK TDS 684B Digital Real Time scope, TEK 11801B scope
Probes	TEK P6247 differential probe, TEK SD-14 probe

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Bill of Materials

Type	Label	Value/Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L TSSOP	DS90LV047ATMTC
IC	U2	(Quad Receiver)	1	16-L TSSOP	DS90LV048ATMTC
Connector	J1, J2	(8-pin RJ45)	2		AMP P/N 558310-1
Resistor	RT1-6	50Ω	6	RC0805	
Resistor	RL1-4	100Ω	4	RC0805	
Resistor	RS1, RS2, RS3, RS4	453Ω	0/4	RC0805	not loaded
Capacitor	CB1, CB2, CB3	0.1µF	3	CC0805	
Capacitor	CB13	0.01µF	1	CC0805	
Capacitor	CB21, CB22, CB23	0.001µF	3	CC0805	
Capacitor	CBR1	10µF, 35V	1	D	Solid Tantalum Chip Capacitor
Headers	J3, J4	3 lead header	2		100 mil spacing (single row header)
Headers	J5, J6, J7, J8	4 lead header	4		100 mil spacing (double row header)
Jumpers		0.1 jumper post shunts	2		
SMB Jack	I4, O4		2	SMB Connector	Johnson P/N 131-3701-201
*SMB Jack or *SMA Jack	I1-3, I5-6, O1-3		0/8	SMB Connector SMA Connector	Johnson P/N 131-3701-201 Johnson P/N 142-0701-201
Plug (banana)	V_{CC}, GND	Uninsulated Standard Pierced Lug Terminal	2		Johnson P/N 108-0740-001
Cable		RJ45 Cable	2		1 meter and 5 meter
Legs			4		
Bolts/washers			4		
PCB			1		LVDS47/48PCB

* Note: On the evaluation board, inputs I1-3, I5-6 and outputs O1-3 are not loaded with connectors. These inputs and outputs can be loaded with either SMBs (P/N 131-3701-201) or SMAs (P/N 142-0701-201).

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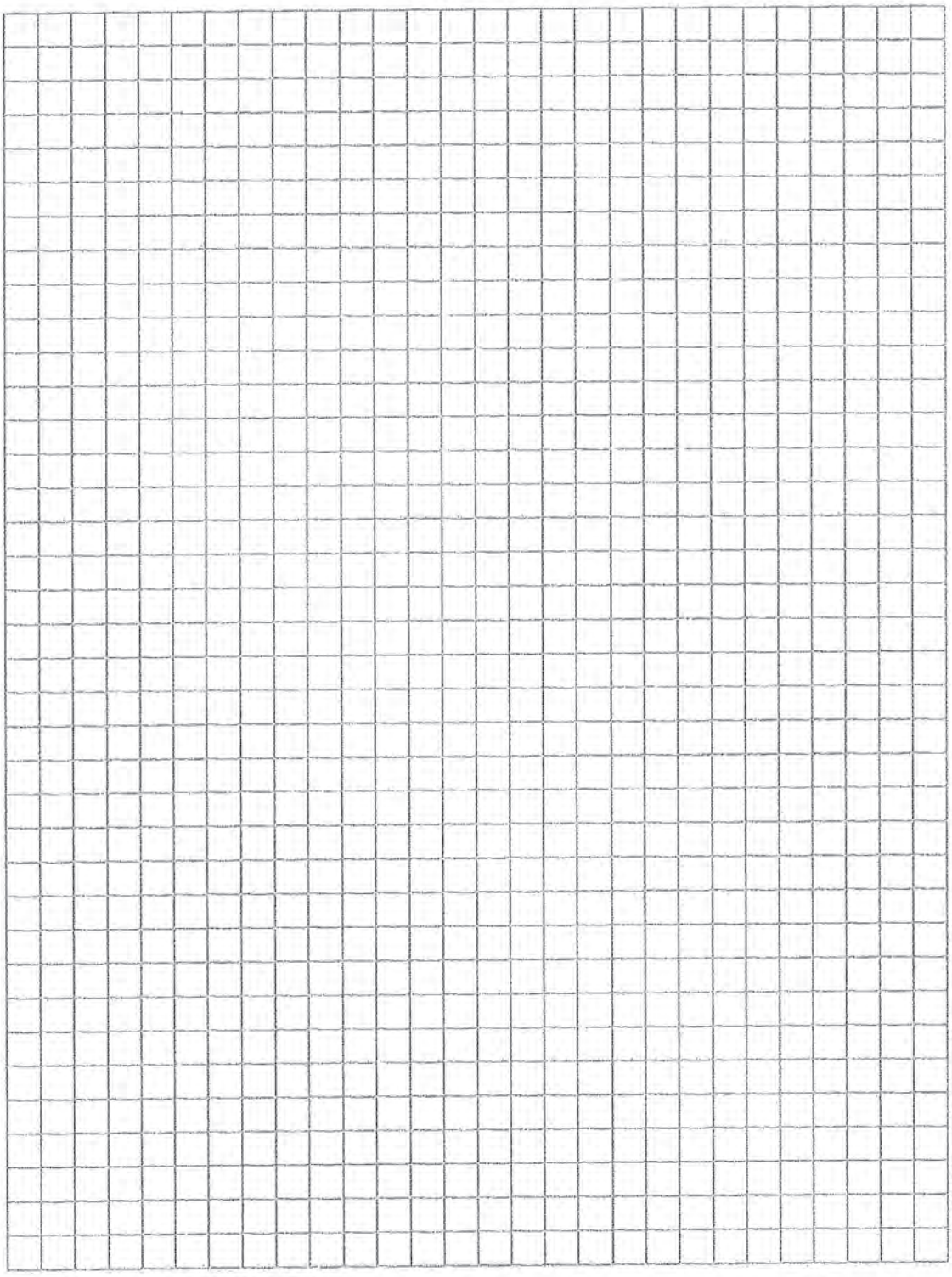

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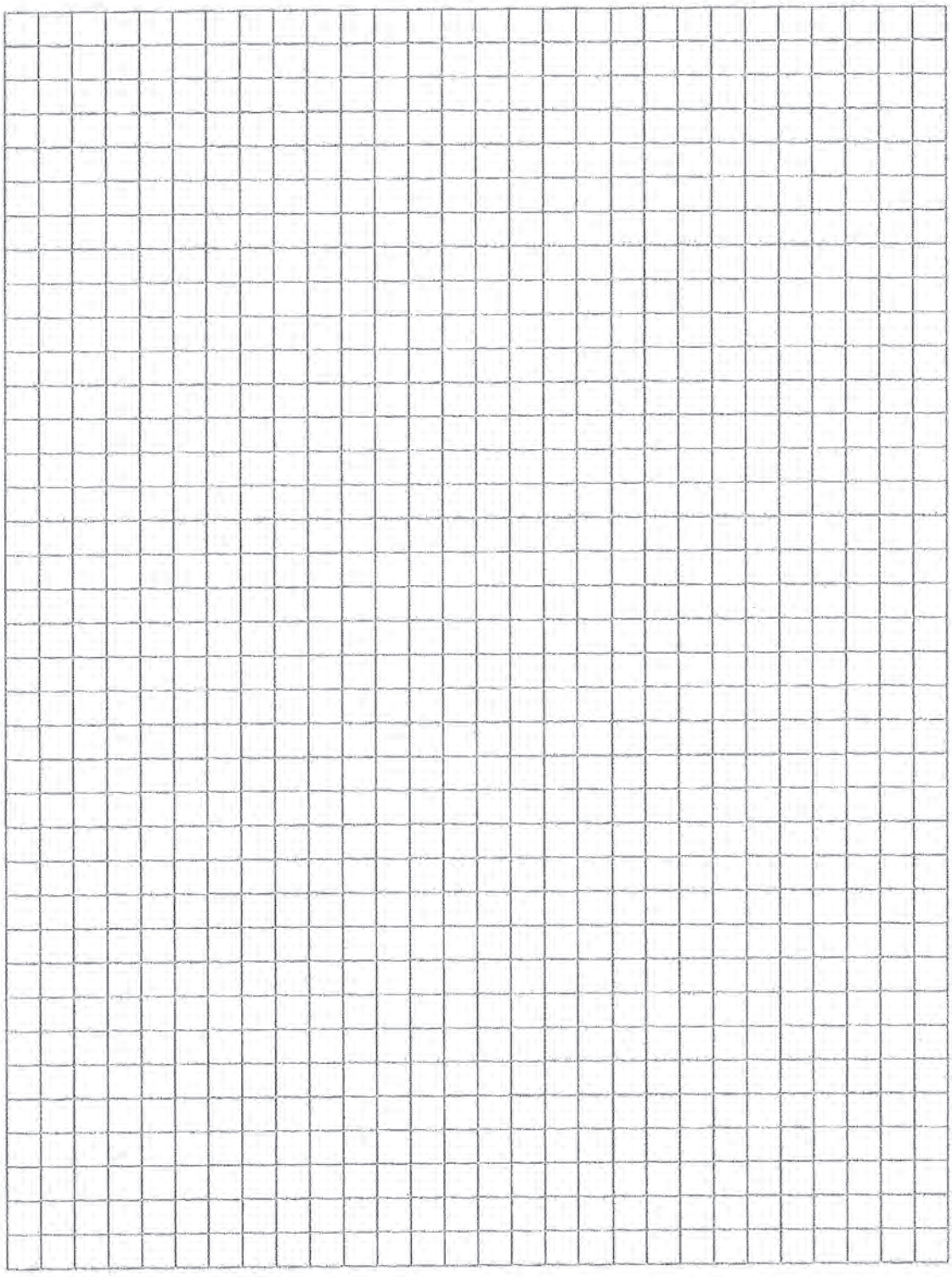

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LVDS Reference

Chapter 8

8.0.0 LVDS REFERENCE – APPLICATION NOTES, STANDARDS, WHITE PAPERS, MODELING INFORMATION AND OTHER DESIGN GUIDES

8.1.0 NATIONAL DOCUMENTS

National also offers more in depth application material on LVDS in the form of application notes, conference papers, white papers and other documents. Please visit the LVDS website for the viewing or downloading of documents. The website's URL is: **www.national.com/appinfo/lvds/**

8.1.1 National LVDS Application Notes

The following application notes on LVDS are currently available:

AN-Number	Topic	Parts Referenced
AN-971	Introduction to LVDS	DS90C031/DS90C032
AN-977	Signal Quality – Eye Patterns	DS90C031
AN-1040	Bit Error Rate Testing	DS90C031/DS90C032
AN-1041	Introduction to Channel Link	DS90CR2xx
AN-1059	Timing (RSKM) Information	DS90CRxxx
AN-1060	LVDS - Megabits @ milliwatts (EDN Reprint)	
AN-1084	Parallel Application of Link Chips	DS90Cxxx
AN-1088	Bus LVDS/LVDS Signal Quality	DS90LV017/27, DS92LV010A
AN-1108	PCB and Interconnect Design Guidelines	DS90CR2xx
AN-1109	Multidrop Application of Channel Links	DS90CR2xx
AN-1110	Power Dissipation of LVDS Drivers and Receivers	DS90C031/2, DS90LV031A/32A
AN-1115	Bus LVDS and DS92LV010A XCVR	DS92LV010A
AN-1123	Sorting Out Backplane Driver Alphabet Soup	

8.1.2 National Application Notes on Generic Data Transmission Topics

National also offers many application notes devoted to the general topics of data transmission, PCB design and other topics pertaining to Interface. A few of these are highlighted below.

AN-Number	Topic
AN-216	An Overview of Selected Industry Interface Standards
AN-643	EMI/RFI Board Design
AN-806	Data Transmission Lines and Their Characteristics
AN-807	Reflections: Computations and Waveforms
AN-808	Long Transmission Lines and Data Signal Quality
AN-912	Common Data Transmission Parameters and their Definitions
AN-916	A Practical Guide to Cable Selection
AN-972	Inter-Operation of Interface Standards
AN-1111	An Introduction to IBIS Modeling

A complete list of all application notes is located at: **http:www.national.com/apnotes/apnotes_all_1.html**

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8.1.3 National Application Notes on Flat Panel Display Link/LVDS Display Interface

A series of application notes is available on the FPD-Link and LDI chipsets. Please see the FPD website for a list of application notes that are currently available at:

www.national.com/appinfo/fpd/

8.1.4 Conference Papers/White Papers from National

The following conference papers are currently available from the LVDS website at:

www.national.com/appinfo/lvds/

- **BLVDS White Paper**
  Signal Integrity and Validation of Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes.
  DesignCon99 Paper
- **BLVDS White Paper**
  A Baker's Dozen of High-Speed Differential Backplane Design Tips.
  DesignCon2000 Paper
- **BLVDS White Paper**
  Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS).
  DesignCon2000 Paper

8.1.5 Design Tools - RAPIDESIGNERS

The National Semiconductor Transmission Line RAPIDESIGNERs make quick work of calculations frequently used in the design of data transmission line systems on printed circuit boards. Based on principles contained in the National Interface Databook, the Transmission Line RAPIDESIGNER benefits from our many years of experience in designing and manufacturing data transmission and interface products and from helping our valued customers obtain the most from National's Interface Products.

The following calculations can be made with the RAPIDESIGNER for both Microstrip and Stripline geometries.

- Characteristic Impedance (Z_O)
- Intrinsic Delay
- Unterminated Stub Length
- Loaded Impedance
- Differential Impedance
- Propagation Delay
- Reflection Coefficient
- C_O and L_O
- Reactance Frequency

Two versions of the popular RAPIDESIGNER are available while supplies last. The two RAPIDESIGNERs differ in the dimensions supported; one is for METRIC units while the other supports ENGLISH units.

- RAPIDESIGNER, Metric Units, LIT# 633200-001
- RAPIDESIGNER, English Units, LIT# 633201-001

A full Operation and Application Guide is provided in AN-905. Also included in the application note are the formulas for the calculations, accuracy information, example calculations and other useful information.

To obtain a RAPIDESIGNER, contact the National Customer Support Center in your area.

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8.2.0 LVDS STANDARD – ANSI/TIA/EIA-644

Copies of the ANSI/TIA/EIA-644 LVDS Standard can be purchased from Global Engineering Documents. Contact information that was current at the time this book was printed is:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704

or call

USA and Canada: 1.800.854.7179
International: 1.303.397.7956

http://global.ihs.com/

8.3.0 IBIS I/O MODEL INFORMATION

I/O Buffer Information Specification (IBIS) is a behavioral model specification defined within the ANSI/EIA-656 standard. LVDS IBIS models are available from National's Website which can be used by most simulators/EDA tools in the industry. Please see: http:www.national.com/models/ibis/Interface/

Also, visit the ANSI/EIA-656 Website: www.eia.org/EIG/IBIS/ibis.htm for a vendor listing or contact your software vendor.

Chapter 13 of National's 1999 Interface Databook (LIT# 400058) describes IBIS models in detail. A major portion of this material is also covered in National's Application Note AN-1111.

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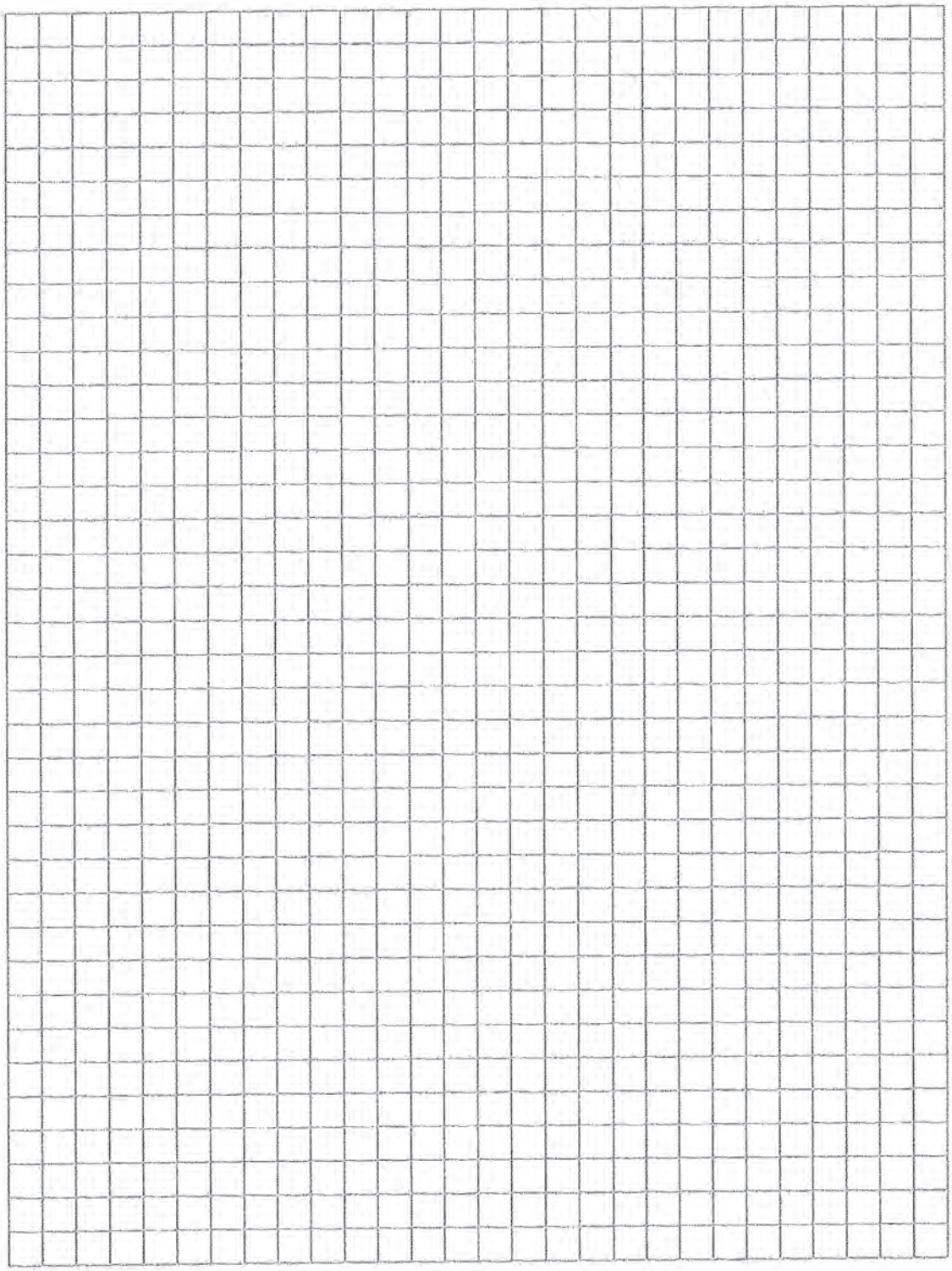

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National's LVDS Website

Chapter 9

9.0.0 LVDS WEBSITE CONTENTS

9.1.0 NATIONAL WEBSITE

National provides an extensive website targeted for Design Engineers and also Purchasing/Component Engineers. From the main page, you can find:

- Product Tree/Selection Guide
- Datasheets
- Application Notes
- Product Folders
  - View/Download: General Descriptions, Features or the Entire Datasheet
  - Product Status and Pricing Information
  - Application Note Reference
- Packaging Information
- Marking Information
- Technical Support
- Search Engine
- Databooks, CD ROMs and Samples

The website's URL is: www.national.com

9.2.0 NATIONAL'S LVDS APPINFO WEBSITE

National provides an in depth application site on LVDS. This site provides the design community with the latest information on National's expanding LVDS family. Please visit the LVDS website to view or download documents. On this site, you can locate:

- LVDS Selection Tables
- Frequently Asked Questions (and Answers)
- Application Note Cross Reference Table (AN Number – Topic – Device ID)
- Interface IBIS Models
- Evaluation Boards – Documentation and Ordering Information
- Family Introductions/Overviews
- Design Tools – RAPIDESIGNERS
- Press Releases

The website's URL is: www.national.com/appinfo/lvds/

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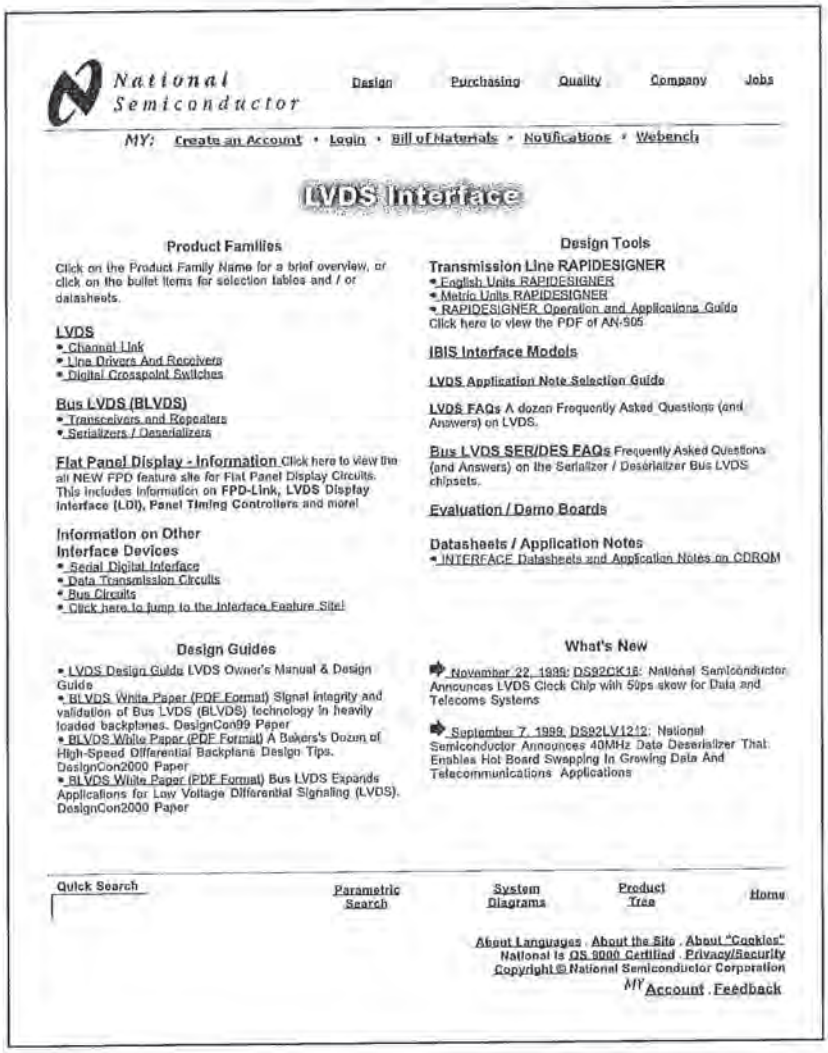

National Semiconductor

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LVDS Interface

Product Families

Click on the Product Family Name for a brief overview, or click on the bullet items for selection tables and / or datasheets.

LVDS
- Channel Link
- Line Drivers And Receivers
- Digital Crosspoint Switches

Bus LVDS (BLVDS)
- Transceivers and Repeaters
- Serializers / Deserializers

Flat Panel Display - Information Click here to view the all NEW FPD feature site for Flat Panel Display Circuits. This includes information on FPD-Link, LVDS Display Interface (LDI), Panel Timing Controllers and more!

Information on Other Interface Devices
- Serial Digital Interface
- Data Transmission Circuits
- Bus Circuits
- Click here to jump to the Interface Feature Site!

Design Tools

Transmission Line RAPIDESIGNER
- English Units RAPIDESIGNER
- Metric Units RAPIDESIGNER
- RAPIDESIGNER Operation and Applications Guide

Click here to view the PDF of AN-905

IBIS Interface Models

LVDS Application Note Selection Guide

LVDS FAQs A dozen Frequently Asked Questions (and Answers) on LVDS.

Bus LVDS SER/DES FAQs Frequently Asked Questions (and Answers) on the Serializer / Deserializer Bus LVDS chipsets.

Evaluation / Demo Boards

Datasheets / Application Notes
- INTERFACE Datasheets and Application Notes on CDROM

Design Guides
- LVDS Design Guide LVDS Owner's Manual & Design Guide
- BLVDS White Paper (PDF Format) Signal integrity and validation of Bus LVDS (BLVDS) technology in heavily loaded backplanes. DesignCon99 Paper
- BLVDS White Paper (PDF Format) A Baker's Dozen of High-Speed Differential Backplane Design Tips. DesignCon2000 Paper
- BLVDS White Paper (PDF Format) Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS). DesignCon2000 Paper

What's New

November 22, 1999: DS92CK16: National Semiconductor Announces LVDS Clock Chip with 50ps skew for Data and Telecoms Systems

September 7, 1999: DS92LV1212: National Semiconductor Announces 40MHz Data Deserializer That Enables Hot Board Swapping In Growing Data And Telecommunications Applications

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Screen shot of LVDS APPINFO website: www.national.com/appinfo/lvds/

9.3.0 OTHER NATIONAL'S APPINFO WEBSITES

9.3.1 "INTERFACE" Products

National provides an application site on INTERFACE. This site provides the design community with the latest information on National's expanding SDI (Serial Digital Interface) and RS-xxx families. Please visit the INTERFACE website to view or download documents.

9.3.2 "FPD" Products

National provides an in depth application site on Flat Panel Display devices. This site provides the design community the latest information on National's expanding FPD-Link, LDI and TCON families. Please visit the FPD website to view or download documents.

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9.3.3 Other/APPINFO/Websites

National provides other in depth application sites. Please visit the main-page for an updated list of pages. This site can be viewed at: **http:www.national.com/appinfo**. It currently includes information on:

- A/D Converters
- Advanced I/O
- Amplifiers
- Audio Products
- Automotive
- Compact RISC
- Custom
- Die Products
- Enhanced Solutions
- Flat Panel Display
- Information Appliance Solutions
- Interface
- LTCC Foundry
- LVDS Interface Products
- Microcontroller
- Micro SMD
- Power
- Scanners
- Temperature Sensors
- USB Technologies
- Wireless Products
- Wireless Basestation Products

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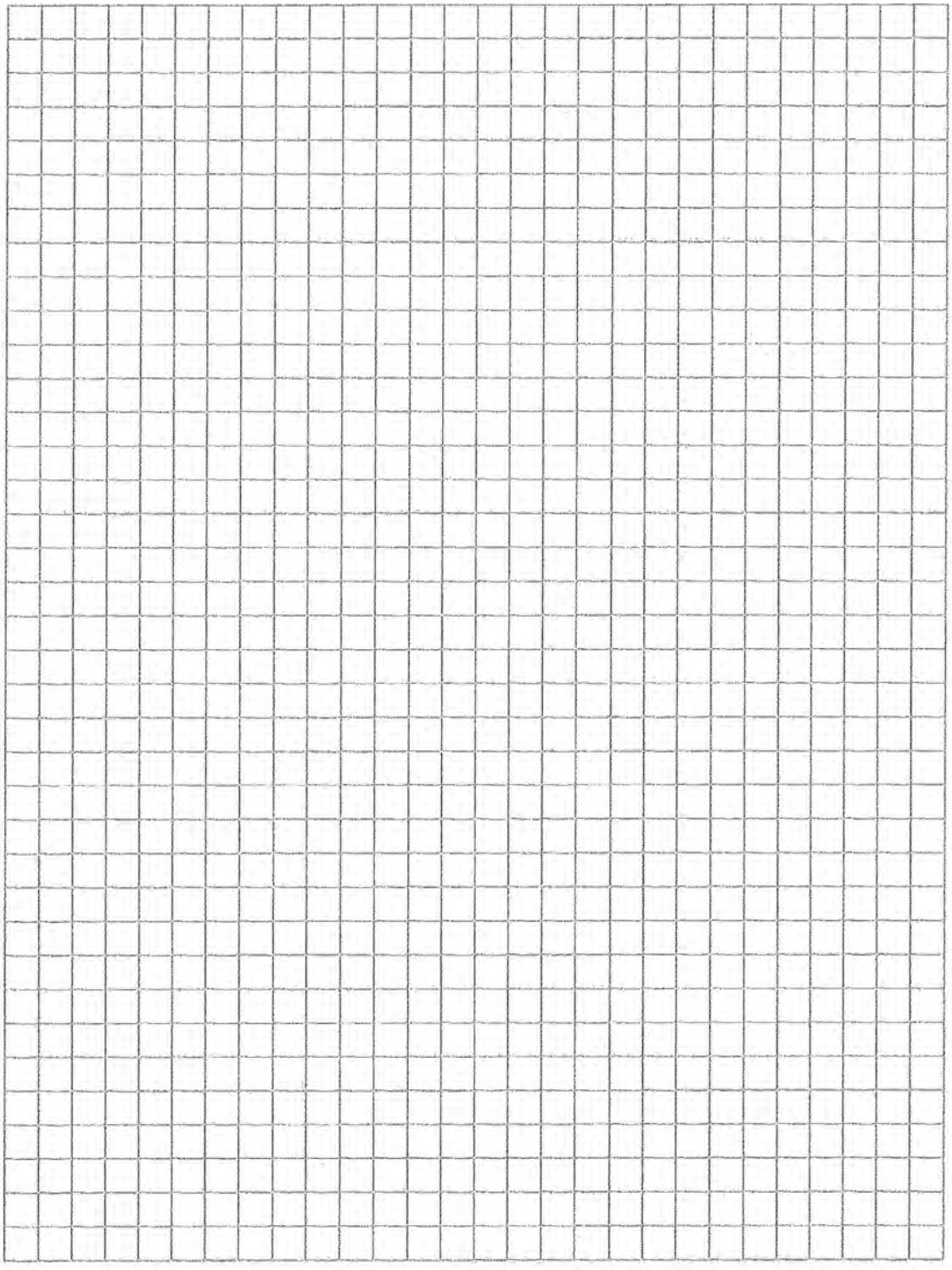

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Glossary, Index and Worldwide Sales Offices

Appendix

GLOSSARY

AN	Application Note
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
B/P	Backplane
BER	Bit Error Rate
BERT	Bit Error Rate Test
BLVDS	Bus LVDS
BTL	Backplane Transceiver Logic
CAT3	Category 3 (Cable classification)
CAT5	Category 5 (Cable classification)
CISPR	International Special Committee on Radio Interference (Comité International Spécial des Perturbations Radioélectriques)
D	Driver
DCR	DC Resistance
DUT	Device Under Test
ECL	Emitter Coupled Logic
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	Enable
ESD	Electrostatic Discharge
EVK	Evaluation Kit
FCC	Federal Communications Commission
FPD	Flat Panel Display
FPD-LINK	Flat Panel Display Link
Gbps	Gigabits per second
GTL	Gunning Transceiver Logic
Hi-Z	High Impedance
IC	Integrated Circuit
I/O	Input/Output
IBIS	I/O Buffer Information Specification
IDC	Insulation Displacement Connector
IEEE	Institute of Electrical and Electronics Engineers
kbps	kilobits per second
LAN	Local Area Network

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GLOSSARY (continued)

LDI	LVDS Display Interface
LVDS	Low Voltage Differential Signaling
Mbps	Mega bits per second
MDR	Mini Delta Ribbon
MLC	Multi Layer Ceramic
NRZ	Non Return to Zero
PCB	Printed Circuit Board
PECL	Pseudo Emitter Coupled Logic
PHY	Physical layer device
PLL	Phase Lock Loop
PRBS	Pseudo Random Bit Sequence
R	Receiver
RFI	Radio Frequency Interference
RS	Recommended Standard
RT	Termination Resistor
RX	Receiver
SCI	Scalable Coherent Interface
SCSI	Small Computer Systems Interface
SDI	Serial Digital Interface
SER/DES	Serializer/Deserializer
SUT	System Under Test
T	Transceiver
TDR	Time Domain Refletometry
TEM	Transverse Electro-Magnetic
TFT	Thin Film Transistor
TI	Totally Irrelevant
TIA	Telecommunications Industry Association
TP	Test Point
TTL	Transistor Transistor Logic
TWP	Twisted Pair
TX	Transmitter
UTP	Unshielded Twisted Pair
VCM	Voltage Common-mode
VCR	Video Cassette Recorder

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